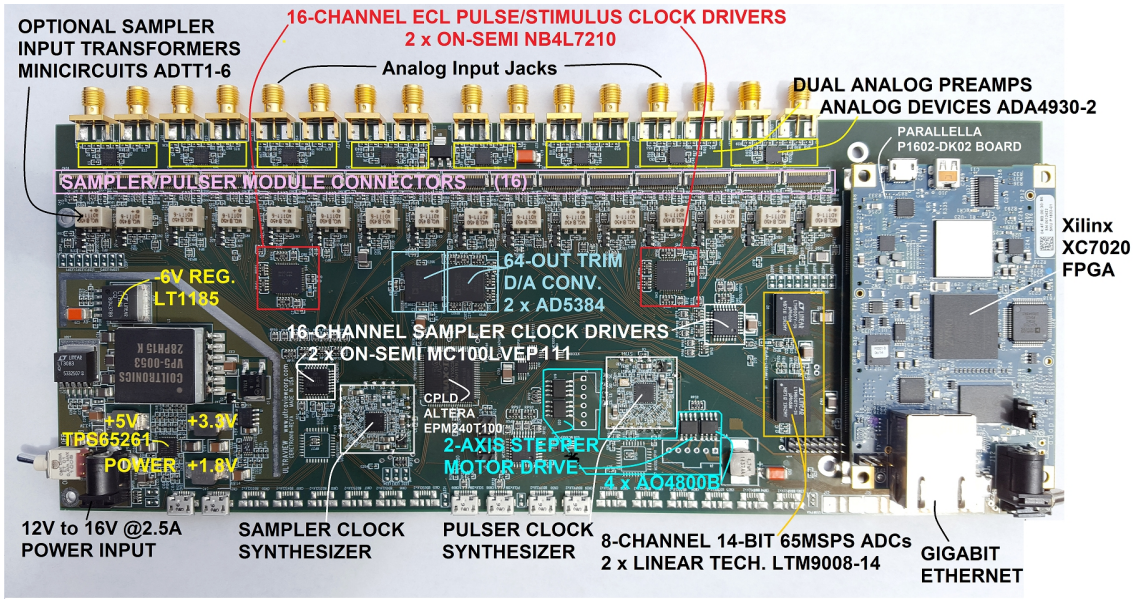
AD14x16-65MSPS-Ethernet

16-channel 14-bit 65MSPS Ethernet-connected DAQ board with signal averaging and stimulus generation



Product Specification – Sept2, 2016
Preliminary

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1. Warranty

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Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation and exclusion may not apply to you. This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

WARNING! To avoid overheating, most Ultraview data acquisition boards must be well cooled. Do not remove supplied heatsinks or fans. Externally supplied airflow may be required on specified models.

2. Description

The AD14-65MSPS-16AVE Ethernet-connected A/D board is designed for demanding large-system uses, in which signals on multiple time-aligned channels need to be observed with high SNR, such as RADAR, nuclear instrumentation, ultrasound, medical imaging, spectroscopy, communications systems, RF component and antenna testing and other critical applications. An on-board low-jitter LMX2581-based RF synthesizer allows any A/D sampling rate between 3.125MSPS and 65MSPS to be software-specified. A second on-board LMX2581 can be programmed to output an optional stimulus clock to four SMA connectors that can drive external transmitters, microwave pulse generators, laser modulators, and other devices.

A special UWB RADAR-optimized version, the AD14-65Mx16AVESTIM, eliminates the 16 SMA analog input connectors and input amps, and instead has 16 20-pin ZIF connectors that accept a wide variety of front-end analog modules, such as transceivers, samplers, pulsed UWB RADAR front ends and nuclear signal conditioners. Each ZIF connector supplies an on-board-generated differential PECL sampling clock that may be set for either 1x or 2x the specified ADC conversion rate, a separately settable differential Tx/pulser clock, +12 to15V and -4 to -12V power, and differential transformer-coupled inputs feeding the slot's respective internal A/D channel.

Based on a hardware averaging engine with near-zero dead-time, implemented in the board's Xilinx™ Zynq7020, the AD14-65Mx16AVE can record concurrent single shot waveforms of up to 4K samples on each of 16 concurrent channels or up to 16K samples/channel on each of 4 concurrent channels. It can additionally perform up to 1024 averages of repetitive signal strings on all 16 channels with record lengths to 4096 samples, in an uninterrupted manner. The precise repetitive acquisition or, alternatively, the summing of each new string of samples onto a running 24-bit average can be triggered by any one of three software-selectable triggering mechanisms:

1. A TTL input, with selectable –/+ slope, which causes each waveforms to be acquired or added to a running average. (coming soon)

2. A software slider-adjustable level on the incoming signal waveform on any of the 16 channels, with specifiable + or – slope, enabling scope-like triggering, with pre-trigger, on a given location on a repeating waveform. (coming soon)

3. Heterodyning trigger input - Triggering will occur on the difference frequency between an optionally specified stimulus frequency and the sampling clock frequency. This is useful for time-of-flight imaging systems, RADAR and pulsed spectroscopy systems, in which transmit or stimulus waveforms are repeated M-times/second and the A/D samples data at a rate of N samples per sec. The result is that the AD14-16Mx16AVE will automatically acquire and/or average complete waveforms that repeat M minus N times per second.

In addition to its averaging and unique triggering modes, which include pre-triggering capability, the AD14-65Mx16AVE is a high dynamic range general purpose high speed data acquisition board capable of transferring acquired data to the host system at up to 60MB/sec (120MB/sec for 2-board/32-channel group, 240MB/sec for 4-board/64 channel group, etc). The precise time alignment of acquisition of all channels to within one sample period, the 24-bit averaging engine, the flexible triggering modes including novel heterodyne trigger, the selectable pre-trigger memory, and the 128-channel expandability, make the AD14-65Mx16AVE uniquely suited for large scientific, nuclear, RADAR, medical imaging and other systems. Moreover, the open-source FPGA firmware and software render this as a viable long-term platform for large-system solution.

As network appliances, AD14-65Mx16AVE boards can be operated from anywhere in the world, enabling coordinated data acquisition at multiple remote and local sites. Data acquisition and display programs are supplied for 64-bit Windows™ 7/8 and Linux6.x/7.x. Either non-averaged or averaged waveforms may be displayed in single-shot or repetitive mode.

3. SPECIFICATIONS

A/D Converter Resolution:	14 bits
Number of Channels:	16 (SMA or ZIF inputs)
SNR:	TBD
SFDR:	TBD
Analog Input Range (SMA jack option):	+/- 500mV (1.0V p-p)
Analog Input Impedance:	50 Ohms || 2 pF
Analog Input Bandwidth (SMA jack option):	DC – 400 MHz
Clock Frequency (ADC):	3.125 MHz – 65 MHz acquisition rates below 12.5MSPS available using averaging
Clock Frequency (Synthesizer):	50MHz – 3.6GHz ADC frequency may be specified to be 1/2, 1/4, 1/8, or 1/16 synthesizer frequency
Clock Frequency (Combined, operational):	3.125 MHz – 65 MHz (below 12.5MHz available using decimation)
Trigger Modes:	TTL, Heterodyne (Synth 1 to Synth 0 difference) Analog Waveform Trigger from any channel
Input connectors:	16 SMA External clock and Trigger inputs
Other Connectors:	Gigabit Ethernet for data and control 8 combination dual clock outputs
Internal DMA transfer rate:	1.6GB/sec
Ethernet transfer rate:	20MB/sec – 80MB/sec, TBD
Operating Temperature Range:	0 to +50 Degrees Celcius
Storage Temperature Range:	-25 to +85 Degrees Celcius
Power Requirements:	+12V to +16V at 5A max
Board size:	10.75” long x 4.261” wide x 0.75” high (including board standoffs).
Required external airflow:	20 lfpm minimum across top of board in any direction

4. Hardware

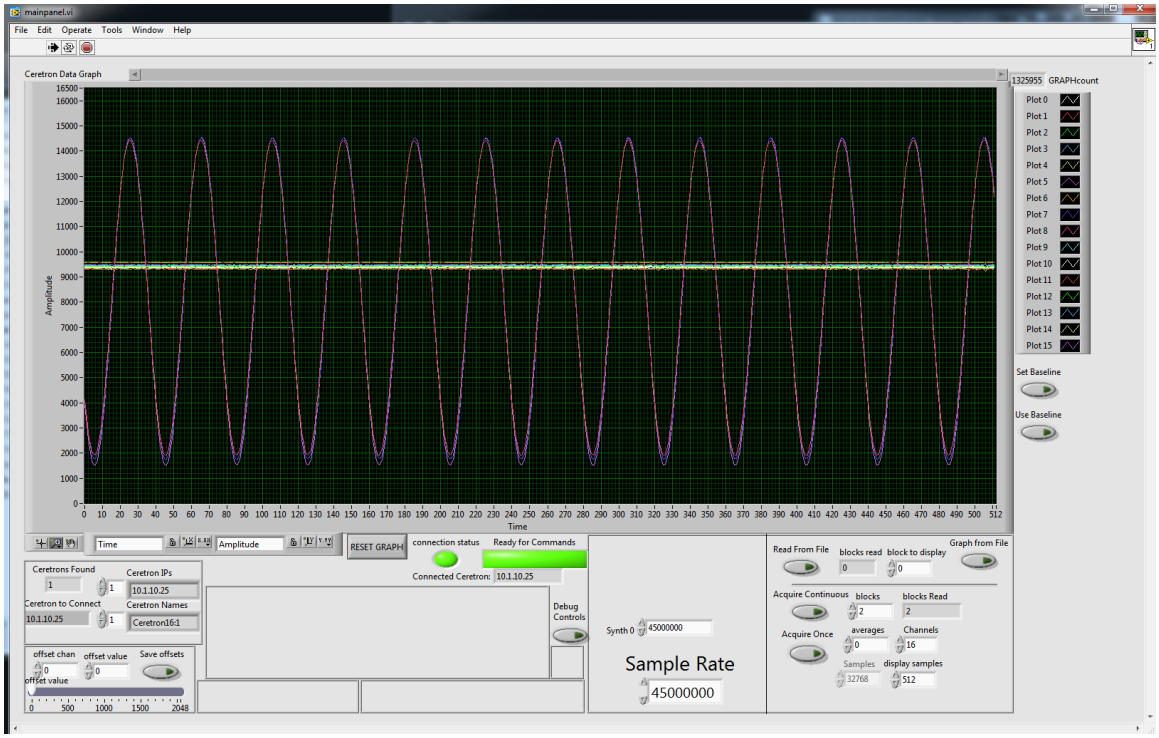
The board consists of a power supply section, 2 ADC's (LTM9008), 2 DAC's (AD5384), 2 drivers (MC100LVEP111) for optional samplers, 2 8-channel independently controllable stimulus clock drivers (NB4L7210), 2 RF Synthesizers (LMX2581), a control CPLD (EPM240T100C3), 8 optional board expansion clock outputs, 1 optional board expansion clock input, and 16 analog inputs. The included, socketed, Parallella boardlet contributes an FPGA (zync 7020), gigabit Ethernet, and an SD card and memory containing the factory supplied operating system (Linux), and server program.

LED's driven by each channel's optional pulser/stimulus power supply input turn on when voltage is applied to Pvcc (LEDP0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15). There are also LED's which indicate the board's various components are working correctly, these will come up upon power up (LED_FPGA, LED_U34). There are also LED's that can be used as debug outputs from the on-board CPLD (LED0,1,2,3,4).

There are two different analog input types the board can accept: bipolar (-500mV to +500mV into 50 ohms) via standard SMA connectors and 20 pin ZIF connectors.

The optional 20 pin ZIF, used on AD14-65Mx16AVESTIM models only, has the following pin usage:
pin 1: Ground
pin 2: 12-15V from on board supply, adjustable via on-board DAC (pulser_v_control)
pin 3: LVPECL Sampler Clock Output (N) (identical for channel slots 0-15)
pin 4: LVPECL Sampler Clock Output (P) (identical for channel slots 0-15)
pin 5: IC_SVG3, adjustable from DAC (identical for channel slots 0-15)
pin 6: IC_SVCT, adjustable from DAC (identical for channel slots 0-15)
pin 7: Sampler Output (P) - signal input to ADC channel for given slot.
pin 8: Sampler Output (N) - signal input to ADC channel for given slot.
pin 9: Pulser Amplitude control – 0 to +5V (independently specifiable signal for each given slot).
pin 10: Pulser Amplitude baseline. Separate output for channels 0-3, 4-7, 8-11, 12-15.
pin 11: Low Reg (0-15)
pin 12: High Reg (0-15)
pin 13: LVPECL Pulser Clock Output (N)
pin 14: LVPECL Pulser Clock Output (P)
pin 15: -6V from on board supply
pin 16: Pulser Vcc, controllable from mux and autosequencer (0-15)
pin 17: IC_PVG3 (0-15)
pin 18: IC_PVCTRLB (0-15)
pin 19: -6V from on board supply
pin 20: Ground

5. LABVIEW™ SOFTWARE (WINDOWS)



Installation:

To install the windows Labview™ software, download and extract the .zip from the Ultraview website at: http://ultraviewcorp.com/downloads.php
You will then need to install the appropriate Labview™ runtime engine package, 2014 64 bit, available at no charge at:
http://www.ni.com/download/labview-run-time-engine-2014/4889/en/

Usage:

Power up the board, and run the client AD14x16_65MSPS.exe. For a single AD14x16 on a local network this can be done in any order. The client will periodically issue a udp broadcast looking for compatible devices on the local network, and any AD14x16 will receive this broadcast and issue a responding broadcast. The client receives this broadcast, identifies the device by IP address, and connects automatically. This will take a second or less once the board has successfully completed its startup sequence.
If more than 1 AD14x16 is on the local network, the client will automatically connect to the first one it finds. However, all devices that are found will show up in the “Ceretron IP's” field, and you can manually type this number into the “ceretron to connect” field. Then the current ceretron must be disconnected by pressing the red stop button in the upper left, this stops the client. The client must then be restarted by pressing the run button in the upper left, 2 icons to the left of the red stop button. The new device will automatically connect as the client restarts. There are two large green status LEDS, one indicates if a connection is established, one indicates if the board is ready to accept commands.
After the device is connected, the acquisition rate can be adjusted by changing the “synth0” field

and/or the “averages” field for manual control, or by changing the “ADC sample rate”. Changing either of these will affect the others. If changing the clock, a recalibrate is necessary and happens automatically, but will take ~2 seconds for the board to be ready for additional commands.

After the software is connected and the clock frequency is set the board is now ready to acquire. The number of averages and number of blocks are passed to the board when the acquire button is pressed. The board will continue to supply data until the number of blocks has been reached, or the connection is broken. Because the ethernet connection has limited bandwidth, certain acquisition schemes will start to lag behind the actual acquisition. If real time performance is crucial, increase the number of averages or decrease the sampling speed until the data rate no longer exceeds the ethernet transfer rate.

A block is 1MB of data, or 512K 2 byte samples. For 1,2,4,8, and 16 channels this corresponds to a record length of 512K, 256K, 128K, 64K, and 32K samples respectively. The sampling data rate is the sampling clock rate times the number of channels (16) times 2 bytes per sample divided by the number of averages. For real time acquisition the sampling data rate cannot exceed the Ethernet transfer rate.

Example: 50MSPS * 2 bytes * 16 channels / 4 averages gives a data rate of 400MB/sec

The averaging engine is an accumulator that adds each 14 bit sample taken from the ADC into a 16 bit accumulator. The accumulator will sum bits in independent bins up to averager length number of samples. It can average up to 4 times.

To stop the acquisition before all the blocks have come in, click the stop button in the upper left, then the run arrow in the upper left to start again. The synth clock frequencies will need to be resent to the board if different than default. The default synth clock settings can be changed on the server component in tcpthread.cpp (see software(advanced)).

Labview has many tools for viewing data in its graph windows, please see https://zone.ni.com/reference/en-XX/help/371361H-01/lvhowto/zooming_on_a_graph_or_char/ for more details.

Medimager only:

There are two controllable clock sources, synthesizers, on the board. Synthesizer 1 controls the ADC clock, while optional synthesizer 0 controls a second clock commonly used with sampler / pulser arrays with a heterodyned trigger. The ADC clock is normally half the synthesizer 1 clock, but can be set to one quarter the synthesizer 1 clock by toggling “ADC 25% clock”. After the rates are set appropriately for your application, press the “change synth frequencies” button. This will set both synthesizers and then recalibrate the ADC for the new clock rate. When it has finished re-calibrating (approximately 2 seconds) the green “ready for commands” LED will illuminate again. For the heterodyned scheme, a recommended rate for synthesizer 0 is suggested when synthesizer 1 has its value changed. This can be sent to the synthesizer 0 field by clicking the toggle switch next to it.

After the software is connected and the clock frequency is set the board is now ready to acquire. The number of averages, averager length, and number of blocks are passed to the board when the acquire button is pressed. The board will continue to supply data until the number of blocks has been reached, or the connection is broken. Because the ethernet connection has limited bandwidth, certain acquisition schemes will start to lag behind the actual acquisition. If real time performance is crucial, increase the number of averages until the data rate no longer exceeds the ethernet transfer rate. Because the board has a very limited amount of on board RAM, if the acquisition gets too far behind the transfer, data will be lost as newer data replaces older data still

waiting to be transferred.

A block is defined as the number of channels (16) times the averager length, with 4 bytes per sample. The sampling data rate is the sampling clock rate times the number of channels (16) times 4 bytes per sample divided by the number of averages. For real time acquisition the sampling data rate cannot exceed the Ethernet transfer rate.

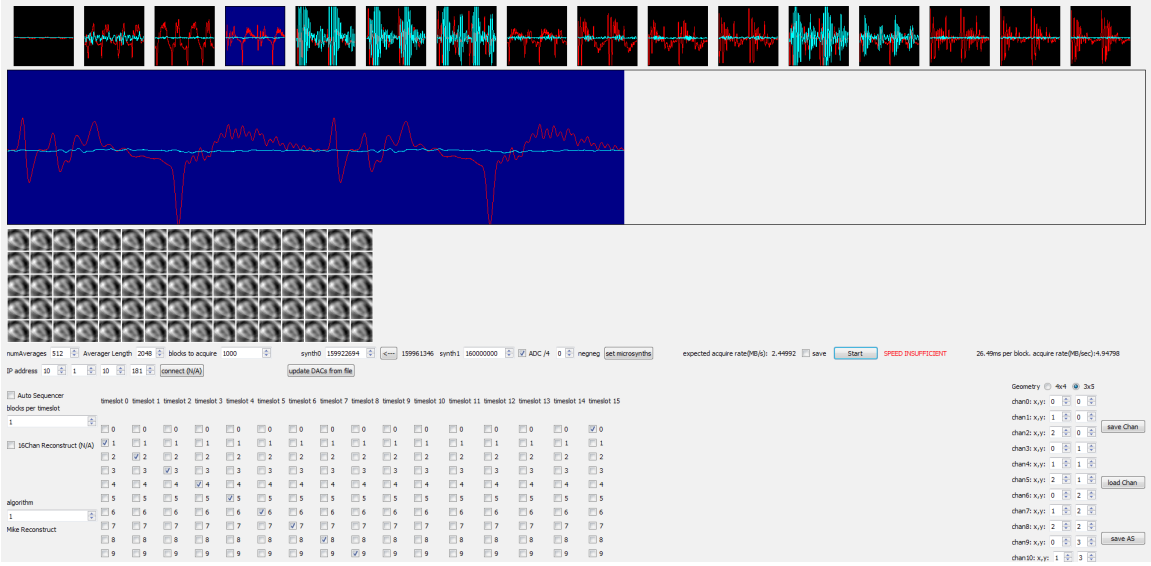
Example: 200MHz synthesizer 0 frequency / 4 = 50MHz ADC clock frequency
50MSPS * 4 bytes * 16 channels / 100 averages gives a data rate of 32MB/sec

The averaging engine is an accumulator that adds each 14 bit sample taken from the ADC into a 32 bit accumulator. The accumulator will sum bits in independent bins up to averager length number of samples. It can average up to 1024 times for a total of 24 bits. For 100 samples given in the example above, the data range of values will be from 0 to 16383*100=1,638,300 for roughly 20.7 bits of precision. Increasing the number of averages for a repeating signal with random noise increases the SNR considerably.

The two DACs on the board control voltage levels sent to various nets to adjust operation. There are 40 channels on each DAC, the ones with currently attached functionality are labeled with their function, and the rest are labeled as their raw output names for potential expansion. The DAC values can be saved to a file (DAC0.txt and DAC1.txt), and are automatically loaded when the program is run.

The channels can be aligned with the offset controls in the bottom left. These values can be saved (offsets.txt), and are automatically loaded when the program is run. Both text files can be edited with notepad or overwritten with new saved values.

6. QT SOFTWARE (LINUX and Windows)



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Installation:

To install the Linux software, download and extract the .zip from the Ultraview website at:
http://ultraviewcorp.com/downloads.php
You will then need to install the Qt 5.6 package from:
http://www.qt.io/download/
Open the Qt project .pro file, then build and run it. A compiler will be necessary, normally gcc is used.

Usage:

This program is functionally similar to the Labview™ program for Windows™. It lacks some of the graphical features, but is multithreaded and features very high throughput. It also has additional image processing options, modifiable by customizing the supplied C code. The raw waveforms from all channels are located at top of the GUI, and any one waveform can be expanded by clicking anywhere in the large open gray area (to deselect all fields), then pushing shift+right and shift+left to select which channel is expanded.

The raw channel output can be saved by clicking the “save” checkbox. The data will be saved to C:\uvdma\data\(date) on windows, and home/uvdma/data/(date) on Linux. Data format is channel 0 sample 0, channel 1 sample 0, channel 2 sample 0... channel 15 sample 0, channel 0 sample 1, channel 0, sample 2... channel 15 sample N. Each value is a 32 bit unsigned int.

This program also has a fully functional hardware auto-sequencer, which allows stimulus to be enabled or disabled for each block of data acquired. To use the auto-sequencer, check the auto sequencer checkbox and select the appropriate channels on the checkboxes below each time slice. Each time slice refers to a single block or multiple blocks of data being collected. If the “blocks per time slice” field is changed from 1 (default) to X, than the auto-sequencer will instead use each time slice to last for X blocks.

This program also features a simple UWB radar image reconstruction algorithm, exact features are still TBD.

7. COMMAND LINE SOFTWARE

The command line software release has both source and executables for the various example programs, which can immediately be run to demonstrate the use of the board, and form an excellent basis for developing your own custom software. The source code for both the command line Linux example programs and the command line Windows example programs share an identical section of cross platform source code (linux still under development). Usage information for the applications is available by simply running the executable without any arguments.

Standard usage: acquireETH 500
This asks for 500 blocks of 1MB each using default parameters

flags:

-IP (address): Enter an IP address to connect to. Necessary if connecting to a remote device, or if multiple devices are on the local network.
-f (filename): change the output file name from uvdma.dat to (filename).
-freq0: Specifies the ADC sample rate
-avg (N): uses N hardware averages. Necessary to acquire at slower speeds than 12.5MHz or to improve SNR.
-chan (N): Channels to acquire from. 1,2,4,8,16 are valid.

Additional features coming soon...

This program can be modified for custom applications. The source is contained in main.cpp and is built using Dev++ (free). The winsock 2 library must be linked to, this is provided in the acquireETH.dev project.

8. SOFTWARE (ADVANCED)

All software for the AD16x14 is open source. The Labview™ client can be edited with the Labview™ development system, and the Qt client can be edited with Qt 5.7. Qt 5.7 is free under a GPL license, but Labview™ must be purchased. In order to recreate the Labview™ executable from the Labview™ project file, the professional Development System version is required. However, the main .vi file can be edited with any version of Labview™, and can run modified code suitable for a wide variety of applications.

In addition to the client interfaces, the server can also be edited. The server component of the AD14x16 resides on the SD card on the parallella board, along with the operating system (Linux) for the parallella. The server is also a Qt based project, and once built can be transferred directly onto the SD card via SSH or SD card reader into the folder “home/parallella”.

There are also two firmware projects, one for the xc7020 FPGA on the parallella board, and one for the CPLD. The source for these projects is available under NDA.

Custom applications for any of the environments (software client, software server, firmware parallella, firmware CPLD) may be requested for an NRE cost. For some OEM applications this cost may be returned to customer in the form of a price reduction for volume deliveries.

9. TROUBLESHOOTING

Problem: Software cannot connect to the board:
Troubleshooting tips:

Have the link lights on the parallella's ethernet port both lit up?
If not, check that the SD card is fully in the socket, and that the board has power.

Do you have an IP address in the ceretron IP's found field?
If you do but cannot connect, the server is either already connected to another client, or not running.

Problem: Ethernet speeds are slow:
Troubleshooting tips:

Has the device correctly autonegotiated a gigabit ethernet link?
If not, check that the router/switch/hub the device is connected to is capable of gigabit.

Is there significant network congestion?
If there is a lot of network traffic, the device may need to be on its own network to maximize performance.

Additional troubleshooting information is displayed on the debug console output from the server. In order to view the debug console output, open up a connection (tera term, SSH), use “top” to locate the process “ad14_16ch”, and use sudo kill “process ID #”. Then run ./ad14_16ch. Now connect using the software as described in sections 5 and 6 and the console will provide debug output from the server. If you are modifying any of the projects, it is a good idea to first observe the normal sequence of operation, as a baseline to compare with the operation of the modified product.

