PCIe Data Acquisition Boards with Ultra-deep RAM and Reconfigurable Virtex 5™ FPGA

Product Specification - July 11, 2013

AD8-3000 Series: 8-bit 3GSPS 2/1-Channel

- AD8-3000x1-8GB; AD8-3000x2-8GB 1 or 2-Chan 3GSPS A/D, 8GB RAM

AD8-1500 Series: 8-bit 1.5 / 3.0GSPS 2-Channel

- AD8-1500x2-8GB 2-Chan 1.5GSPS A/D, 8GB RAM
  Also operable as single channel 3GSPS A/D

AD12-1800 Series: 12-bit 1.5GSPS 2-Channel

- AD12-1800x2-8GB 2-Chan 1800MSPS A/D, 8GB RAM
  Also operable as single channel 3.6GSPS A/D

AD12-2000 Series: 12-bit 2GSPS 2-Channel

- AD12-2000x2-8GB 2-Chan 2GSPS A/D, 8GB RAM
  Also operable as single channel 4GSPS A/D

AD14-400 Series: 14-bit 400MSPS 2-Channel

- AD14-400x2-8GB 2 Chan 400MSPS A/D, 8GB RAM
  Includes Zero Dead-Time Hardware Averaging

AD14-500 Series: 14-bit 500MSPS 2-Channel

- AD14-500x2-8GB 2 Chan 500MSPS A/D, 8GB RAM
  Includes Zero Dead-Time Hardware Averaging

AD16-250 Series: 16-bit 250MSPS 4/2-Channel

- AD16-250x2-8GB; AD16-250x4-8GB 2 or 4-Chan 250MSPS A/D, 8 GB RAM
  Includes Zero Dead-Time Hardware Averaging

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1. Warranty

Ultraview Corporation hardware, software and firmware products are warranted against defects in materials and workmanship for a period of two (2) years from the date of shipment of the product. During the warranty period Ultraview Corporation shall at its option, either repair or replace hardware, software or firmware products which prove to be defective. Ultraview products are only supported with Ultraview provided firmware and software, any modifications made by customers are not supported and are not covered under warranty. This limited warranty does not cover damage caused by misuse or abuse by customer, and specifically excludes damage caused by dropping the unit or by the application of excessive voltages to the inputs and/or outputs of data acquisition boards. Due to the complex nature of computer systems, Ultraview boards operation should be verified in the desired host computer system prior to purchasing multiple units of host system. For example in some systems the reset time is too short to allow certain Ultraview FPGA-based boards to fully configure before being accessed by the system, therefore requiring a warm boot before operation is possible in these systems.

While Ultraview Corporation hardware, software and firmware products are designed to function in a reliable manner, Ultraview Corporation does not warrant that the operation of the hardware, software or firmware will be uninterrupted or error free. Ultraview products are not intended for use as critical components in life support systems, aircraft, military systems or other systems whose failure to perform can reasonably be expected to cause significant injury to humans. Ultraview expressly disclaims liability for loss of profits and other consequential damages caused by the failure of any product, and recommends that customer purchase spare units for applications in which the failure of any product would cause interruption of work or loss of profits, such as industrial, shipboard or military equipment. In no way will Ultraview Corporation's liability exceed the amount paid by the customer for the product.

This limited warranty is in lieu of all other warranties expressed or implied. The warranties provided herein are buyer's sole remedies. In no event shall Ultraview Corporation be liable for direct, special, indirect, incidental or consequential damages suffered or incurred as a result of the use of, or inability to use these products. This limitation of liability remains in force even if Ultraview Corporation is informed of the possibility of such damages.

Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation and exclusion may not apply to you. This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

WARNING! To avoid overheating, all Ultraview boards must be installed in a well-cooled

workstation or server chassis, or alternatively in an industrial chassis PC. Installation in a PC or workstation without fans at the front end of the card cage may cause the board to overheat, and resulting damage is not covered by warranty. A minimum of 100 linear feet per minute airflow is required for model AD14-400x2 boards.

2. Series Descriptions

Ultraview's PCIe data acquisition boards are complete high-speed data acquisition systems on a single full-size PCI-express (PCIe) card. Designed for low jitter operation in military, scientific, medical and industrial applications these boards function in PCIe systems having at least one free x16 PCIe slot. Drivers and ready-to-use user programs for Linux (RedHat Enterprise 5.0™ (RHEL) 64-bit, and Centos 6.2 64-bit) and 32-bit/64-bit Windows Vista™ and XP™ are provided. **Windows 7/8 64-bit drivers are signed.** Disabling driver signature is no longer necessary.

The digital section of the these boards includes a Xilinx Virtex 5™ FPGA, which queues up the A/D data in its FIFO registers, and outputs bursts of 128-bit wide LVDS data vectors at up to 500 MWPS (8GB/sec) that are transferred into two 4GB DDR DIMM modules capable of storing up to 8GB of A/D input data. Between these forward bursts of A/D data, the FPGA can burst read data to the PCIe bus interface, allowing for uninterrupted high speed data acquisition. These devices require x16 PCIe slots but are only wired for x8 lane operation. Sustained transfer rate to the host is approximately 1.4 GB/s, and is determined by the speed of this 8 lane PCIe interface, which is dependent on the motherboard, the operating system and applications running. All 14-bit boards in this line have a selective recording input (Trigger Input) that allows the user to start and stop acquisition in response to an external TTL input.

All boards support host uploading of new firmware, allowing users to reprogram the on-board Xilinx Virtex 5 FPGA. Supplied software reads the device's configuration space, re-programs the FPGA's boot PROM, loads the FPGA, and re-instantiates the device's configuration space. Reconfiguration time is typically 2-10 minutes.

The FPGA on all boards is an 1136 pin Xilinx Virtex 5™. Any 1136 pin Virtex 5™ FPGA may be specified by the customer at the time the board is ordered, these include the XC5VLX50T, XC5VLX110T, XC5VLX155T, and XC5VSX95T. **The default FPGA is an XC5VLX50T™** whose registers and BRAMS are approximately 20% (40% registers and 60% BRAMS for AD14-500 and AD16-250 series) occupied when the board is shipped, larger FPGA's are shipped using significantly less of these resources. With the purchase of any Ultraview data acquisition system, and under the protection of a signed Non-Disclosure Agreement, Ultraview Corporation will provide the VHDL firmware source code to allow its OEM users the option of loading their own firmware into the on-board FPGA. Please request a copy of Ultraview Corporation's NDA for specifics by e-mailing sales@ultraviewcorp.com. Portions of the VHDL including the PCIe bus controller and DRAM controller are not included as HDL source code, they are provided as core net-lists.

All boards are full-size PCIe boards (4.2” x 8.625”). **Due to the excess height of the memory modules on the board each board occupies the space of two slots.**

To avoid overheating, all boards must be installed either in well-cooled workstation or server chassis. Installation in a standard PC chassis is feasible as long as a minimum of 100 linear feet per minute of airflow is provided to cool the board. Further, the filler bracket for the slot in front of the Ultraview board (the slot into which the Ultraview's DIMMs protrude) must be removed to allow additional airflow to the board.

2.1 AD8-3000x1 or x2 8-Bit Single or Dual Channel 3GSPS A/D

AD8-3000 models contain one or two 3 GSPS 8-bit A/D converters, 8GB of on-board DDR2 DRAM memory and the ability to transfer data directly into the computer system's memory at approximately 1400 MB/s. A/D sampling may either be controlled by an external clock input between 500 MHz and 1500 MHz (which will cause sampling at 1000 to 3000MHz respectively) or the 1000MHz on-board internal clock that allows sampling at 2GSPS. Multiple boards may be configured to acquire either concurrently, for more simultaneous acquisition channels, or sequentially, for longer record length. ECL triggering is available for edge-triggering the start of data acquisition using the Sync A/D SMA jack on AD8-3000 RevB and RevC boards or the Trigger/Sync SMA jack on AD8-3000 RevD boards. A proper ECL trigger signal is a 0V to 0.5V-1.2V positive-going edge with a rise time less than 2ns. Selective recording and TTL Triggering for RevC and RevB boards can be driven directly from an SMA on the card. For RevD boards, a 26-pin connector and TTL Input Panel will be provided which the user can driver from an SMA. See Appendix for more details. A proper selective recording signal is a TTL signal with levels describe in Section 3. Specifications – AD8-3000/AD8-1500. Selective recording is defaulted as an active LOW (board has an internal pull-down resistor, leave unconnected if unused).and can be specified to an active high. Decimation up to x16 is available.

A novel active/passive input BALUN on the AD8-3000 models allows frequencies down to DC to be acquired, while retaining the low noise characteristics of a transformer coupled front-end at higher frequencies, up to 2 GHz.

2.2 AD8-1500x2 8-Bit Dual Channel 1.5GSPS / 1 Channel 3.0GSPS A/D

AD8-1500 models contain two 1.5 GSPS 8-bit A/D converters, 8GB of on-board DDR2 DRAM memory and the ability to transfer data directly into the computer system's memory at approximately 1400 MB/s. A/D sampling may either be controlled by an external clock input between 500 MHz and 1500 MHz (which will cause sampling at 500 to 1500MHz respectively) or the 1000MHz on-board internal clock that allows sampling at 1GSPS. Multiple boards may be configured to acquire either concurrently, for more simultaneous acquisition channels, or sequentially, for longer record length. The AD8-1500x2 may be set, under software control, to operate either as a dual channel 1500 MSPS board or a single channel 3 GSPS board. ECL triggering is available for edge-triggering the start of data acquisition using the Trigger/Sync SMA jack on AD8-1500 boards. A proper ECL trigger signal is a 0V to 0.5V-1.2V positive-going edge with a rise time less than 2ns. Selective recording and TTL Triggering for RevC and RevB boards can be driven directly from an SMA on the card. For RevD boards, a 26-pin connector and TTL Input Panel will be provided which the user can drive from an SMA. See Appendix for more details. Decimation up to x16 is available.

A novel active/passive input BALUN on the AD8-1500x2 models allows frequencies down to DC to be acquired, while retaining the low noise characteristics of a transformer coupled front-end at higher frequencies, up to 2GHz.

2.3 AD12-1800x2 12-Bit Dual Channel 1.8GSPS / 1 Channel 3.6 GSPS A/D

Models in the AD12-1800 series contain a dual 1800 MSPS 12-bit A/D converter, 8GB of on-board DDR2 DRAM memory and the ability to transfer data directly into the computer system's memory at approximately 1.4 GB/s. A/D sampling may either be controlled by an external clock input between 300 MHz and 1800 MHz (the A/D sampling rate is equal to the clock frequency) or the 1000MHz on-board internal clock (available via an SMA jack). Multiple boards may be

configured to acquire either concurrently, for more simultaneous acquisition channels, or sequentially, for longer record length. Two TTL inputs are also sampled concurrently with each analog input and stored along with the A/D data. A 26-pin connector and TTL Input Panel will be provided which the user can drive from an SMA. See Appendix for more details. Decimation up to x8 is available.

ECL triggering is available for edge-triggering the start of data acquisition using the Trigger/Sync SMA jack. A proper ECL trigger signal is a 0V to 0.5V-1.2V positive-going edge with a rise time less than 2ns.

The AD12-1800x2-8GB may also be configured to acquire a single 12-bit channel at any clock frequency between 300MSPS and 3.6 GSPS. A novel active/passive input BALUN on the AD12-1500x2 models allows frequencies down to DC to be acquired, while retaining the low noise characteristics of a transformer coupled front-end at higher frequencies, up to 2GHz.

2.4 AD12-2000x2 12-Bit Dual Channel 2GSPS / 1 Channel 4GSPS A/D <Preliminary>

Models in the AD12-2000 series contain a dual 2GSPS 12-bit A/D converter, 8GB of on-board DDR2 DRAM memory and the ability to transfer data directly into the computer system's memory at approximately 1.4 GB/s. A/D sampling may either be controlled by an external clock input between 300 MHz and 2GHz (the A/D sampling rate is equal to the clock frequency) or the 1000MHz on-board internal clock (available via an SMA jack). Multiple boards may be configured to acquire either concurrently, for more simultaneous acquisition channels, or sequentially, for longer record length. Two TTL inputs are also sampled concurrently with each analog input and stored along with the A/D data. A 26-pin connector and TTL Input Panel will be provided which the user can drive from an SMA. See Appendix for more details. Decimation up to x8 is available.

ECL triggering is available for edge-triggering the start of data acquisition using the Trigger/Sync SMA jack. A proper ECL trigger signal is a 0V to 0.5V-1.2V positive-going edge with a rise time less than 2ns.

The AD12-2000x2-8GB may also be configured to acquire a single 12-bit channel at any clock frequency between 300MSPS and 4 GSPS. A novel active/passive input BALUN on the AD12-1500x2 models allows frequencies down to DC to be acquired, while retaining the low noise characteristics of a transformer coupled front-end at higher frequencies, up to 2GHz.

2.5 AD14-400x2 Dual Channel 14-bit 400MSPS A/D w/Hardware Averaging

Models in the AD14-400 series contain two 400 MSPS 14-bit A/D converters, 8GB of on-board DDR2 DRAM memory and the ability to transfer data directly into the computer system's memory at approximately 1.4 GB/s. A/D sampling may either be controlled by an external clock input between 20 MHz and 400 MHz (the A/D sampling rate is equal to the clock frequency) or the 400MHz on-board internal clock (available via an SMA jack). Multiple boards may be configured to acquire either concurrently, for more simultaneous acquisition channels, or sequentially, for longer record length. Four TTL inputs are also sampled concurrently with the analog input and stored along with the A/D data. Both channels on the AD14-400x2-8GB sample concurrently at a rate equal to the input clock frequency. Selective recording / acquire disable can be used to record data on either the high or low of a user specified signal. A proper selective recording signal is a TTL signal with levels describe in Section 5. Specifications - AD14-400. Selective recording is defaulted as an active LOW (board has an internal pull-down resistor, leave

unconnected if unused).and can be specified to an active high. Fiducial marks can be added with to easy mark the samples recorded during each high or low phase.

Hardware averaging, with near-zero dead-time, is implemented in the board's Xilinx™ FPGA, the upgraded AD14-400-8GB-50T and AD14-400-8GB-155T (boards shipped after (2/26/2013) can average repetitive signal strings up to 1 million times with record lengths to 16384 samples (-50T model) and 262144-samples (-155T model) uninterrupted. The precise repetitive summing of each new string of samples onto a running 32-bit average can be triggered by any one of three software-selectable triggering mechanisms:

- A TTL input, with selectable –/+ slope, causes waveforms to be acquired or added to a running average.

- A software slider-adjustable level on the incoming signal waveform on any of the 4 channels, with + or – slope, enabling scope-like triggering, with pre-trigger, on a given place on a repeating waveform.

While all AD14-400x2-8GB models contain 8GB of on-board memory, if averaging is selected, the averager length on AD14-400x2-8GB-50T is 16384 samples in single channel mode, or 8192 samples on each channel in dual channel mode. On AD14-400x2-8GB-155T, the averager length is up to 131072 samples in single channel mode, or up to 65536 samples on each channel in dual channel mode.

2.6 AD14-500x2 Dual Channel 14-bit 500MSPS A/D w/Hardware Averaging

Models in the AD14-500 series contain two 500 MSPS 14-bit A/D converters, 8GB of on-board DDR2 DRAM memory and the ability to transfer data directly into the computer system's memory at up to 1.4GB/s. A/D sampling may either be controlled by an external clock input between 80 MHz and 500 MHz (the A/D sampling rate is equal to the supplied external clock frequency) or the 500MHz on-board internal clock. Multiple boards may be configured to acquire either concurrently, for more simultaneous acquisition channels, or sequentially, for longer record length. Both channels on the AD14-500x2-8GB sample concurrently at a rate equal to the input clock frequency (500MSPS when internal clock is specified, or 80-500MSPS when a 80MHz to 500 MHz external clock is supplied). Selective recording / acquire disable can be used to record data on either the high or low of a user specified signal. A selective recording signal is a TTL signal 0V to 3V. Selective recording is defaulted as an active low, but can be specified to an active high.

Hardware averaging, with near-zero dead-time, is implemented in the board's Xilinx™ FPGA, the ULTRADYNE14-500Mx2AVE-8GB-50T/155T and ULTRADYNE14-500x4AVE-8GB-50T/155T can each average repetitive signal strings up to 1 million times with record lengths to 16384 samples (-50T model) and 262144-samples (-155T model) uninterrupted. The precise repetitive summing of each new string of samples onto a running 32-bit average can be triggered by any one of three software-selectable triggering mechanisms:

- A TTL input, with selectable –/+ slope, causes waveforms to be acquired or added to a running average.

- A software slider-adjustable level on the incoming signal waveform on any of the 4 channels, with + or – slope, enabling scope-like triggering, with pre-trigger, on a given place on a repeating waveform.

- Heterodyning trigger input - Triggering will occur on the difference frequency between this input and the sampling clock frequency. This is useful for time-of-flight imaging

systems, RADAR and pulsed spectroscopy systems, in which transmit or stimulus waveforms are repeated M-times/second and the A/D samples data at a rate of N samples per sec. The result is that the ULTRADYNE14 will automatically acquire and/or average complete waveforms that repeat M minus N times per second.

While all ULTRADYNE AD14-500 models contain 8GB of on-board memory, if averaging is selected, the averager length on ULTRADYNE 14-500x2AVE-8GB-50T is 16384 samples in single channel mode, or 8192 samples on each channel in dual channel mode. On ULTRADYNE 14-500x2AVE-8GB-155T, the averager length is up to 131072 samples in single channel mode, or up to 65536 samples on each channel in dual channel mode.

2.7 AD16-250 Dual or Quad channel 16-bit 250MSPS A/D with Hardware Averaging

Models in the AD16-250 series contain two or four 250 MSPS 16-bit A/D converters, 8GB of on-board DDR2 DRAM memory and the ability to transfer data directly into the computer system's memory at up to 1.4GB/s. A/D sampling may either be controlled by an external clock input between 20 MHz and 250 MHz (the A/D sampling rate is equal to the supplied external clock frequency) or the 250MHz on-board internal clock. Multiple boards may be configured to acquire either concurrently, for more simultaneous acquisition channels, or sequentially, for longer record length. All channels on the AD16-160x2-8GB sample concurrently at a rate equal to the input clock frequency (250MSPS when internal clock is specified, or 40-250MSPS when a 40MHz to 500 MHz external clock is supplied). Selective recording / acquire disable can be used to record data on either the high or low of a user specified signal. A proper selective recording signal is a TTL signal 0V to 3V. Selective recording is defaulted as an active low, but can alternatively be specified to an active high.

Hardware averaging, with near-zero dead-time, is implemented in the board's Xilinx™ FPGA. The ULTRADYNE16-250Mx2AVE-8GB-50T/155T and ULTRADYNE16-250x4AVE-8GB-50T/155T can each average repetitive signal strings up to 1 million times with averaged record lengths to 16384 samples (-50T model) and 262144-samples (-155T model) uninterrupted. The precise repetitive summing of each new string of samples onto a running 32-bit average can be triggered by any one of three software-selectable triggering mechanisms:

- A TTL input, with selectable –/+ slope, causes waveforms to be acquired or added to a running average.

- A software slider-adjustable level on the incoming signal waveform on any of the 4 channels, with + or – slope, enabling scope-like triggering, with pre-trigger, on a given place on a repeating waveform.

- Heterodyning trigger input - Triggering will occur on the difference frequency between this input and the sampling clock frequency. This is useful for time-of-flight imaging systems, RADAR and pulsed spectroscopy systems, in which transmit or stimulus waveforms are repeated M-times/second and the A/D samples data at a rate of N samples per sec. The result is that the ULTRADYNE16 will automatically acquire and/or average complete waveforms that repeat M minus N times per second.

While all ULTRADYNE AD16-250 models contain 8GB of on-board memory, if averaging is selected, the averager length on ULTRADYNE 16-250x2AVE-8GB-50T is 16384 samples in single channel mode, or 8192 samples on each channel in dual channel mode. On ULTRADYNE 16-250x2AVE-8GB-155T, the averager length is up to 131072 averaged samples in single channel mode, or up to 65536 averaged samples on each channel in dual channel mode.

On ULTRADYNE 16-250x4AVE-8GB-50T models, the averager length is16384 samples in single channel mode, 8192 averaged samples on each channel in dual channel mode, or 4096 samples on each sample in 4-channel mode. On ULTRADYNE 16-250x4AVE-8GB-155T models, the averager length is 131072 averaged samples in single channel mode, 65536 samples on each channel in dual channel mode, or 32768 averaged samples on each sample in 4-channel mode.

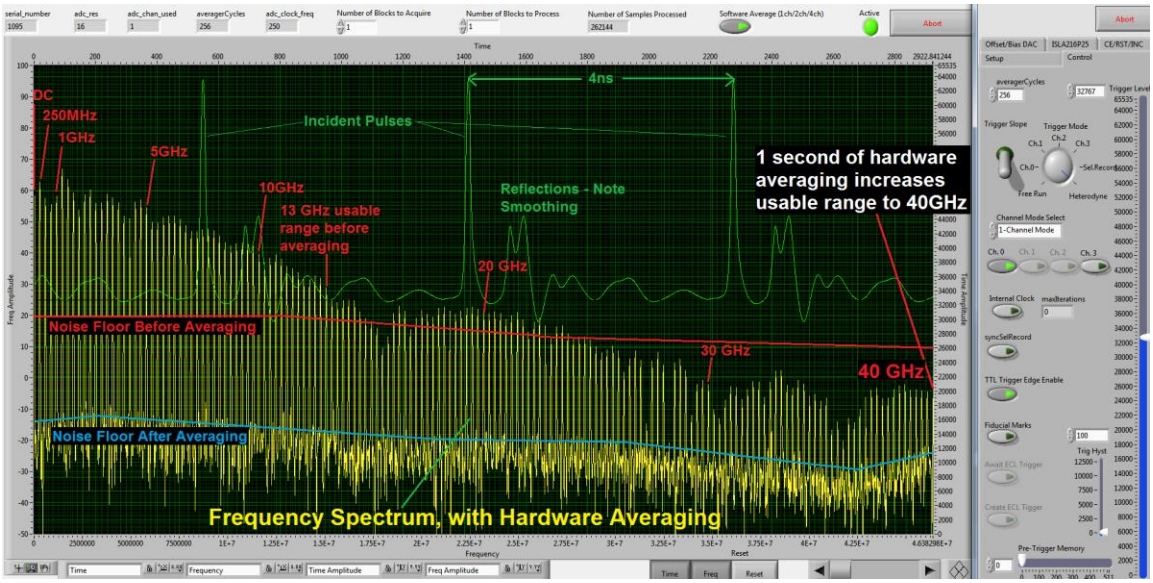


Figure 1. Ultradyne16-250x2 fed by a Libove-Chacko 40GHz microwave sampler/pulser TDR spectrometer, displaying the reflection spectrum of a microwave bowtie antenna excited by a repeating 15 picosecond 250 million pulse/second train. Entire DC-40GHz spectrum (yellow trace) is captured with 120dB dynamic range, using under 1 second of hardware averaging, at nearly 100% collection efficiency**.** Averaged waveforms, despite containing antenna pickup of ambient RFI are so stable that they appear static. Heterodyne trigger **automatically triggers the board at the difference frequency (250.290 MPPS pulse frequency sampled at 250MSPS) to coherently average 290,000 waveforms per second**.

3. Specifications – AD8-3000 / AD8-1500

A/D Converter Resolution:	8 Bits
SNR: AD8-3000:	42 dB (70MHz Input, 2000 MSPS, 1MB FFT) /
AD8-1500:	46 dB (70MHz Input, 1000 MSPS, 1MB FFT)
SFDR: AD8-3000:	48 dB (70MHz Input, 2000 MSPS, 1MB FFT) /
AD8-1500:	57 dB (70MHz Input, 1000 MSPS, 1MB FFT)
Analog Input Range:	-350mV to +350mV **Do not exceed +/-800mV**
Analog Input Impedance:	50 ohms || 2pF
Analog Input Bandwidth (-3dB BW):	DC to 3 GHz / DC to 2 GHz
Sampling Rate into on-board RAM:	
Maximum:	3000 MSPS / 1500MSPS
Minimum:	128 MSPS / 64 MSPS (rates <1000MSPS / 500MSPS use decimation) Decimation: x1 (none), x2, x4,x8,x16
Clock Input (AC Coupled)	
Frequency: AD8-3000:	500MHz – 1500MHz (1/2 the sampling rate)
AD8-1500:	500MHz – 1500MHz (1x the sampling rate)
Input Impedance:	50 ohms in series with 0.01uF
AC Voltage Minimum:	0.3V Peak-to-Peak
AC Voltage Maximum:	1.0V Peak-to-Peak **DC voltage must not exceed +/- 5V**
Optional Sync ECL Input (AC coupled) : (Trigger/Sync or Sync A/D SMA jack)	Positive-going edge - rise time must be <2ns 0.5V p-p min, 1.2V p-p max.
Trigger Modes (software selectable):	1) Start immediately upon software command 2) Wait for externally supplied ECL trigger
Optional (Selective Recording) TTL Input: (Acquire disable SMA jack)	Vil: 0V min, 0.4V max, Vih: 2.4V min, 3.3V max. 0V - 3.0V **Do not exceed 3.2V**
DMA Transfer Rate:	1.4 GB/s (host system dependent)
Operating Temperature Range:	0 to +50 Degrees Celsius
Storage Temperature Range:	-25 to +85 Degrees Celsius
Power Requirements (board occupies 2 slots):	+3.3V +/-5% at 2.6A Typ. (3.0A Max) +12V +/-5% at 1.2A Typ. (1.5A Max)

4. Specifications - AD12-1800x2 (Preliminary Specification)

A/D Converter Resolution:	12 Bits
Number of Channels:	2 at up to 1.8GSPS or 1 at up to 3.6GSPS
Signal-to-Noise Ratio:	61 dB
Spurious Free Dynamic Range:	75 dBc (typ)
Analog Input Range:	+/-375mV (750mVpp) **Do not exceed +/-1V**
Analog Input Impedance:	50 ohms || 2pF
Analog Input Bandwidth	DC to 1.6 GHz (-3dB BW)
Sampling Rate into on-board RAM:	
Maximum:	1800 MSPS (3.6GSPS into single channel)
Minimum:	300 MSPS (dual channel mode) 600 MSPS (single channel mode) (rates <600MSPS / 300MSPS use decimation) Decimation: x1 (none), x2, x4,x8
Clock Input (AC Coupled)	
Frequency	300MHz – 1500MHz
Input Impedance:	50 ohms in series with 0.01uF
AC Voltage Minimum:	0.7V Peak-to-Peak
AC Voltage Maximum:	4.0V Peak-to-Peak **DC voltage must not exceed +/- 5V**
Optional Trigger (Selective Recording) Input:	0V - 3.3V **Do not exceed 3.3V**
Trigger Modes (software selectable):	1) Start immediately upon software command 2) Wait for externally supplied ECL trigger
DMA Transfer Rate:	~1.5 GB/s (host system dependent)
Operating Temperature Range:	0 to +50 Degrees Celsius
Storage Temperature Range:	-25 to +85 Degrees Celsius
Power Requirements (board occupies 2 slots):	+3.3V +/-5% at 3.3A Max (2.6 A typical) +12V +/-5% at 3.0A Max (2.0 A typical)

5. Specifications - AD12-2000x2 (Preliminary Specification)

A/D Converter Resolution:	12 Bits
Number of Channels:	2 at up to 2GSPS or 1 at up to 4GSPS
Signal-to-Noise Ratio:	61 dB
Spurious Free Dynamic Range:	75 dBc (typ)
Analog Input Range:	+/-375mV (750mVpp) **Do not exceed +/-1V**
Analog Input Impedance:	50 ohms || 2pF
Analog Input Bandwidth	DC to 1.6 GHz (-3dB BW)
Sampling Rate into on-board RAM:	
Maximum:	2 GSPS (4GSPS into single channel)
Minimum:	300 MSPS (dual channel mode) 600 MSPS (single channel mode) (rates <600MSPS / 300MSPS use decimation) Decimation: x1 (none), x2, x4,x8
Clock Input (AC Coupled)	
Frequency	300MHz – 2GHz
Input Impedance:	50 ohms in series with 0.01uF
AC Voltage Minimum:	0.7V Peak-to-Peak
AC Voltage Maximum:	4.0V Peak-to-Peak **DC voltage must not exceed +/- 5V**
Optional Trigger (Selective Recording) Input:	0V - 3.3V **Do not exceed 3.3V**
Trigger Modes (software selectable):	1) Start immediately upon software command 2) Wait for externally supplied ECL trigger
DMA Transfer Rate:	~1.5 GB/s (host system dependent)
Operating Temperature Range:	0 to +50 Degrees Celsius
Storage Temperature Range:	-25 to +85 Degrees Celsius
Power Requirements (board occupies 2 slots): +12V +/-5% at 3.0A Max (2.0 A typical)	+3.3V +/-5% at 3.3A Max (2.6 A typical)

6. Specifications – AD14-400x2

A/D Converter Resolution:	14 Bits
Number channels:	2, Simultaneously sampled
Signal-to-Noise Ratio	70 dB (70MHz Input, 400 MSPS, 1MB FFT)
SFDR	74 dB (70MHz Input, 400 MSPS, 1MB FFT)
Analog Input Range:	+/-375mV (750mVpp) **Do not exceed +/-1V**
Analog Input Impedance:	50 ohms || 2pF
Analog Input Bandwidth	DC to 1.4 GHz (-3dB BW)
Sampling Rate into on-board RAM:	
Maximum:	400 MSPS
Minimum:	20 MSPS
Clock Input (AC Coupled)	
Frequency	20MHz – 400MHz
Input Impedance:	50 ohms in series with 0.01uF
AC Voltage Minimum:	0.7V Peak-to-Peak
AC Voltage Maximum:	4.0V Peak-to-Peak **DC voltage must not exceed +/- 5V**
Optional Trigger (Selective Recording) Input:	0V - 3.3V **Do not exceed 3.3V**
Trigger Modes (software selectable):	1) Start immediately upon software command 2) Wait for externally supplied TTL trigger
DMA Transfer Rate:	~1.4 GB/s (host system dependent)
Operating Temperature Range:	0 to +50 Degrees Celsius
Storage Temperature Range:	-25 to +85 Degrees Celsius
Power Requirements (board occupies 2 slots):	+3.3V +/-5% at (2.6A Typ.) (3.0A Max) +12V +/-5% at (1.2A Typ.) (1.5A Max) .

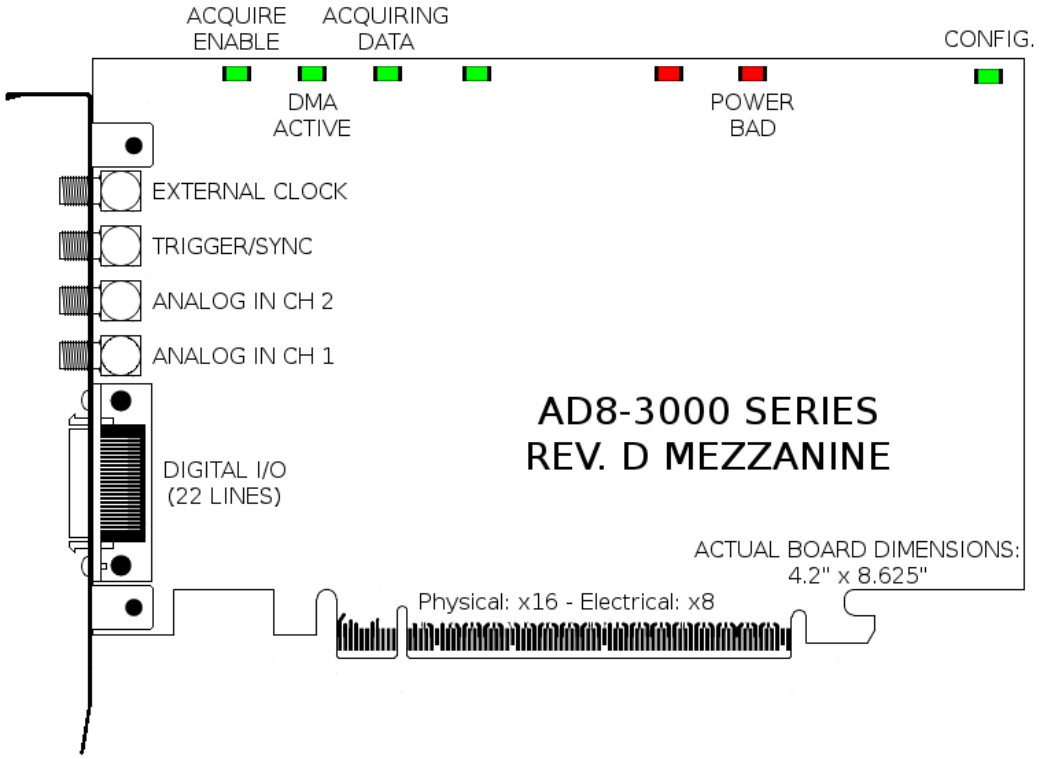
7. Specifications – AD14-500x2

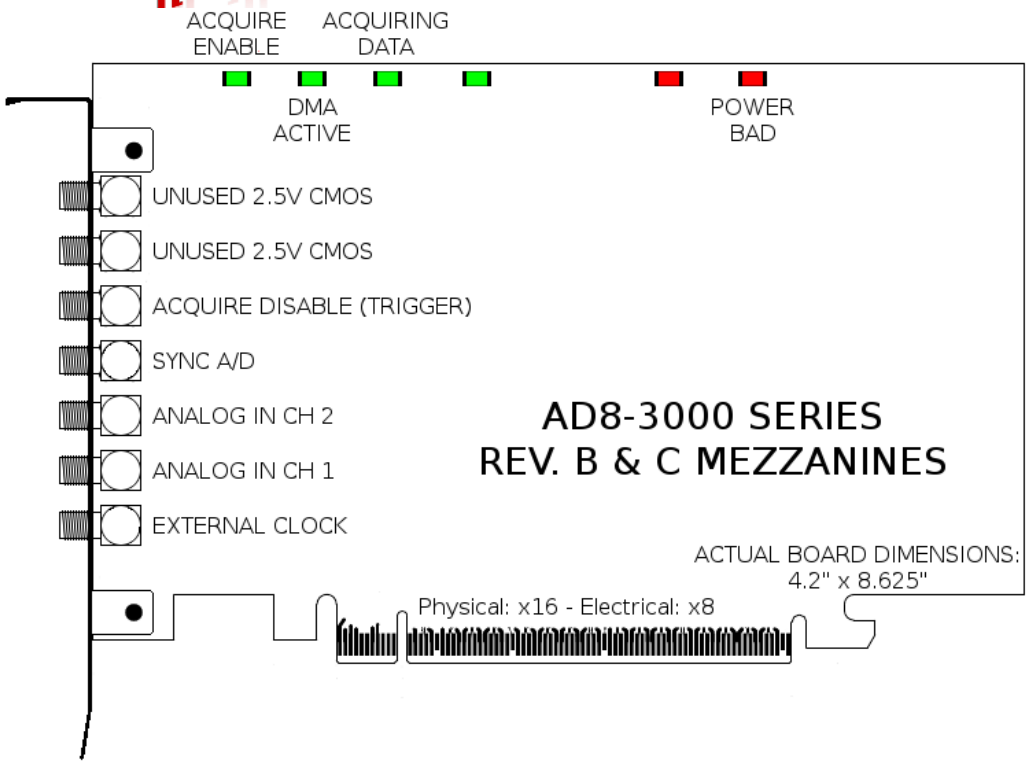
A/D Converter Resolution:	14 Bits
Number of Channels:	2, Concurrently sampled
Signal-to-Noise Ratio	Approx. 73 dB
Dynamic Range:	Approx. 85 dB (w/o Hardware Averaging) Up to 140 dB (w/ 1sec. of Hardware Averaging)
SFDR	Approx. 84 dB @30MHz
Analog Input Range:	+/-375mV (750mVpp) **Do not exceed +/-1.5V**
Analog Input Impedance:	50 ohms || 2pF
Analog Input Bandwidth	DC to 300 MHz (-3dB BW)
Sampling rate into on-board RAM:	
Maximum:	500 MSPS
Minimum:	80 MSPS
Clock Input (AC Coupled)	
Frequency	80MHz – 500MHz
Input Impedance:	50 ohms in series with 0.01uF
AC Voltage Minimum:	0.5V Peak-to-Peak
AC Voltage Maximum:	1.2V Peak-to-Peak **DC voltage must not exceed +/- 5V**
Optional Trigger (Selective Recording) Input:	0V – 2.5V **Do not exceed 3.3V**
Trigger Modes (software selectable):	1) Start immediately upon software command 2) Wait for externally supplied TTL trigger 3) Heterodyne mode – trigger on difference frequency between sampling clock and external stimulus clock
Input connectors:	**4 MMCX female jacks. Board is shipped with four 4-foot MMCX-male to SMA-male cables.**
DMA Transfer Rate:	~1.4 GB/s (host system dependent)
Operating Temperature Range:	0 to +50 Degrees Celsius
Storage Temperature Range:	-25 to +85 Degrees Celsius
Power Requirements (board occupies 2 slots):	+3.3V +/-5% at 3.3A Max (2.6 A typical) +12V +/-5% at 2.0A Max for 4GB

8. Specifications – AD16-250x2, AD16-250x4

A/D Converter Resolution:	16 Bits
Number of Channels:	2, Concurrently sampled (Model: AD16-250x2) 4, Concurrently sampled (Model: AD16-250x4)
Signal-to-Noise Ratio	Approx. 77 dB
Dynamic Range:	Approx. 88 dB (w/o Hardware Averaging) Up to 160 dB (w/ 2sec. of Hardware Averaging)
SFDR	Approx. 87 dB @30MHz
Analog Input Range:	+/-375mV (750mVpp) **Do not exceed +/-1.5V**
Analog Input Impedance:	50 ohms || 2pF
Analog Input Bandwidth	DC to 200 MHz (-3dB BW)
Sampling rate into on-board RAM:	
Maximum:	250 MSPS
Minimum:	40 MSPS
Clock Input (AC Coupled)	
Frequency	40MHz – 250MHz
Input Impedance:	50 ohms in series with 0.01uF
AC Voltage Minimum:	0.5V Peak-to-Peak
AC Voltage Maximum:	1.2V Peak-to-Peak **DC voltage must not exceed +/- 5V**
Optional Trigger (Selective Recording) Input:	0V – 2.5V **Do not exceed 3.3V**
Trigger Modes (software selectable):	1) Start immediately upon software command 2) Wait for externally supplied TTL trigger 3) Heterodyne mode – trigger on difference frequency between sampling clock and external stimulus clock
Input connectors:	**4 MMCX female jacks. Board is shipped with four 4-foot MMCX-male to SMA-male cables.**
DMA Transfer Rate:	~1.4 GB/s (host system dependent)
Operating Temperature Range:	0 to +50 Degrees Celsius
Storage Temperature Range:	-25 to +85 Degrees Celsius
Power Requirements (board occupies 2 slots):	+3.3V +/-5% at 3.3A Max (2.6 A typical) +12V +/-5% at 2.0A Max for 4GB

9. AD8-3000/AD8-1500 Series Cable I/O and LEDs Diagram





9.1 AD8-3000 / AD8-1500 Cable Description

External Clock A single frequency clock must be continuously supplied before any user programs are run. This external clock is useful if acquisition is to be synchronized to an external source. For applications in which an external clock is not desired, the board's internal clock can be used instead, the software must select internal clock mode, **and the external clock input jack must be left unconnected**.

Analog In 2, Analog In 1 The SMA analog input connectors accept a single-ended voltage in the range specified in the specifications section, under no circumstances should the signal supplied to the analog input exceed the specified range as damage may occur that is not covered by the warranty. Both Analog In 2 and Analog In 1 are concurrently sampled, and their precise time-alignment make them well suited for I/Q sampling.

Acquire Disable (Trigger) This is the TTL trigger or selective recording input available only on Rev B and Rev C boards. The board will store data to the on-board RAM only when the acquire disable input is LOW (board has an internal pull-down resistor, leave unconnected if unused). The timing in this mode is not precise to a single sample and can vary from 0 to 3 samples if the input is not synchronized with the A/D clock.

Sync A/D This input is used on earlier mezzanines to externally unreset the ADCs ensuring that multiple boards have aligned digital data. This take an ECL trigger. A proper ECL trigger signal is a 0V to 0.5V-1.2V positive-going edge with a rise time less than 2ns.

Trigger/Sync This edge-triggered input is used on Rev D and later mezzanines to both unreset the ADCs and trigger acquisition. It is an AC-coupled input that should be driven by a positive-going edge with a swing of approximately 1V. This takes an ECL trigger. A proper ECL trigger signal is a 0V to 0.5V-1.2V positive-going edge with a rise time less than 2ns.

9.2 AD8-3000 / AD8-1500 LED Description

Acquire Enable Indicates that the board is armed for acquisition and will store data when the user requests this by means a software command and optional external trigger.

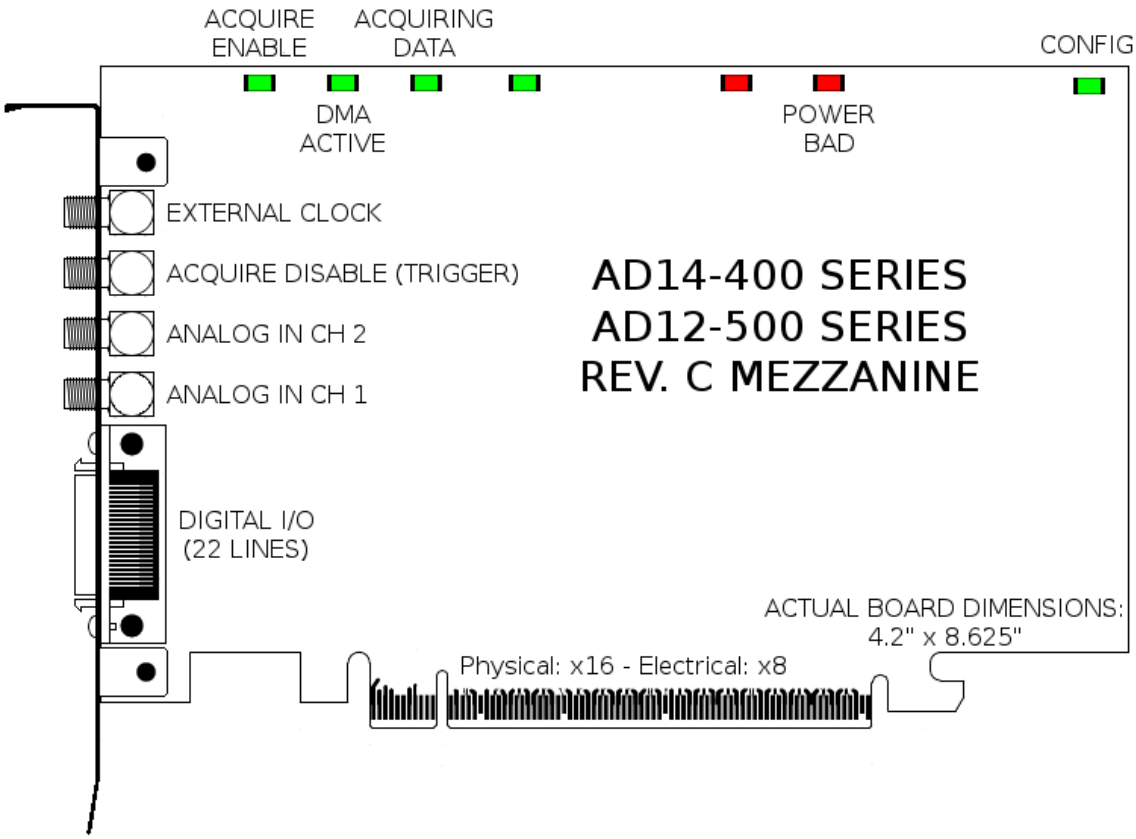
Acquiring Data Indicates the board is currently storing data to its local memory.

DMA Active Indicates the board is performing DMA transfers to the host system. As the boards can concurrently acquire to the on-board dual-ported memory, and DMA to host, both this and the Acquiring Data LED will often be lit concurrently.

Power Bad Indicates the DC power to the DRAM and ADCs is out of spec. This may occur if a fault develops in the board's power supply, or if the host slot in which it is installed is incapable of supplying sufficient current to power the board.

Config Indicates the board's FPGA is properly configured.

10. AD12-1800 / AD12-2000 / AD14-400 Series Cable I/O and LEDs



10.1 AD12-1800 / AD12-2000 / AD14-400 Cable Description

External Clock A single frequency clock must be continuously supplied before any user programs are run. This external clock is useful if acquisition is to be synchronized to an external source. For applications in which an external clock is not desired, the board's internal clock can be used instead, the software must select internal clock mode, and the external clock input must be left unconnected.

Analog In 2, Analog In 1 The SMA analog input connectors accept a single-ended voltage in the range specified in the specifications section, under no circumstances should the signal supplied to the analog input exceed the specified range as damage may occur that is not covered by the warranty. Both Analog In 2 and Analog In 1 are concurrently sampled, and their precise time-alignment make them well suited for I/Q sampling.

Acquire Disable (Trigger) This is the trigger or selective recording TTL input. The board will store data to the on-board RAM only when the acquire disable input is LOW (board has an internal pull-down resistor, leave unconnected if unused). The timing in this mode is not precise to a single sample and can vary from 0 to 3 samples if the input is not synchronized with the A/D clock.

TTL Input 0 This TTL input, available on earlier mezzanines, is sampled and stored along with the analog inputs.

10.2 AD12-1800 / AD12-2000 / AD14-400 LED Description

Acquire Enable Indicates that the board is armed for acquisition and will store data when the user requests this by means a software command and optional external trigger.

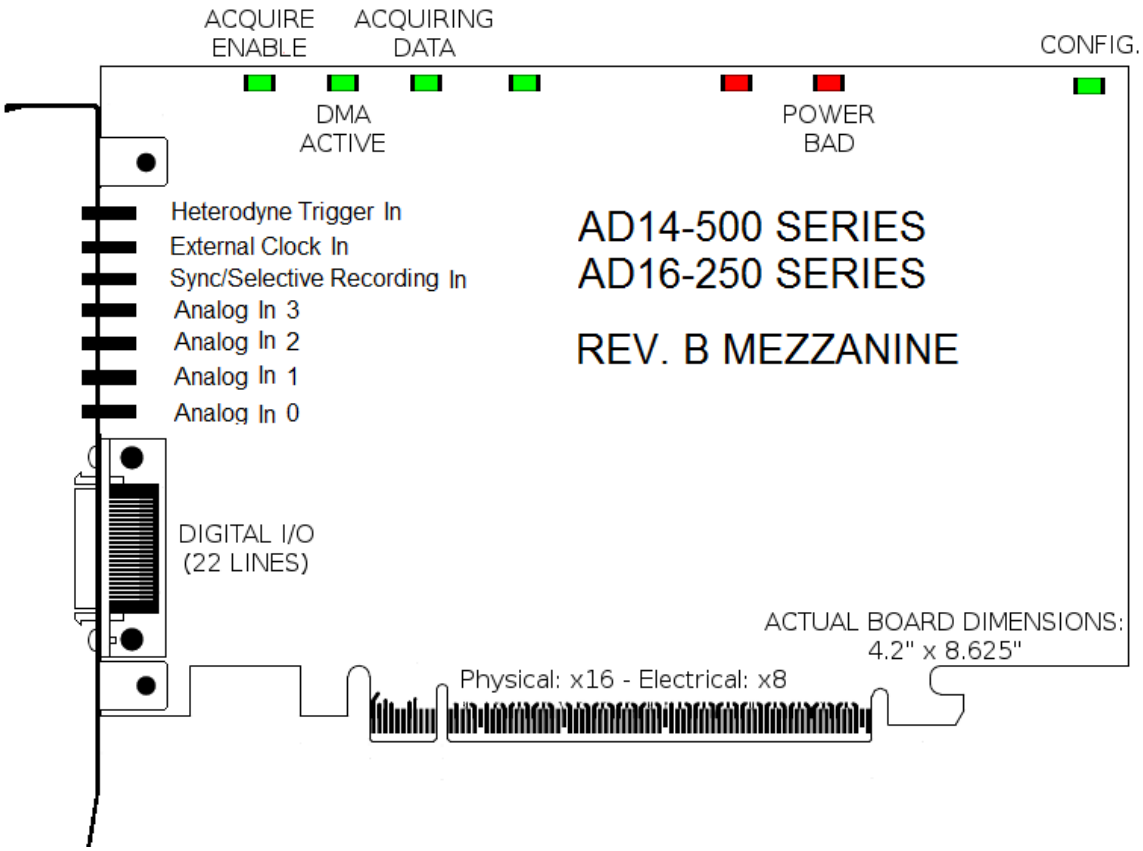
Acquiring Data Indicates the board is currently storing data to its local memory.

DMA Active Indicates the board is performing DMA transfers to the host system. As the boards can concurrently acquire to the on-board dual-ported memory, and DMA to host, both this and the Acquiring Data LED will often be lit concurrently.

Power Bad Indicates the DC power to the DRAM and ADCs is out of spec. This may occur if a fault develops in the board's power supply, or if the slot in which it is installed is incapable of supplying sufficient current to power the board.

Config Indicates the board's FPGA is properly configured.

11. AD14-500 / AD16-250 Series Cable I/O and LEDs



11.1 AD14-500 / AD16-250 Cable Description

Heterodyne Trigger In A heterodyning sine wave input. Triggering will automatically occur on the difference frequency between this input and the sampling clock frequency. This is useful for time-of-flight imaging systems, RADAR/LIDAR and pulsed spectroscopy systems, in which transmit or stimulus waveforms are repeated M-times/second and the A/D samples data at a rate of N samples per second. The result is that the ULTRADYNE16 board will automatically acquire and/or average complete waveforms that repeat M minus N times per second.

External Clock In A single frequency clock must be continuously supplied before any user programs are run. This external clock is useful if acquisition is to be synchronized to an external source. For applications in which an external clock is not desired, the board's internal clock can be used instead, the software must select internal clock mode, and the external clock input must be left unconnected.

Sync/ Selective Recording In This is the trigger or selective recording TTL input. The board will store data to the on-board RAM only when the acquire disable input is LOW (board has an internal pull-down resistor, leave unconnected if unused). The timing in this mode is not precise to a single sample and can vary from 0 to 3 samples if the input is not synchronized with the A/D clock.

Analog In 3, Analog In 2, **Analog In 1, Analog In 0** The SMA analog input connectors accept a single-ended voltage in the range specified in the specifications section, under no circumstances should the signal supplied to the analog input exceed the specified range as damage may occur that is not covered by the warranty. All Analog Ins are concurrently sampled, and their precise time-alignment makes them well suited for I/Q sampling.

11.2 AD14-500 / AD16-250 LED Description

Acquire Enable Indicates that the board is armed for acquisition and will store data when the user requests this by means a software command and optional external trigger.

Acquiring Data Indicates the board is currently storing data to its local memory.

DMA Active Indicates the board is performing DMA transfers to the host system. As the boards can concurrently acquire to the on-board dual-ported memory, and DMA to host, both this and the Acquiring Data LED will often be lit concurrently.

Power Bad Indicates the DC power to the DRAM and ADCs is out of spec. This may occur if a fault develops in the board's power supply, or if the slot in which it is installed is incapable of supplying sufficient current to power the board.

Config Indicates the board's FPGA is properly configured.

12. Hardware Installation and Setup

Handle the board carefully – mechanical damage to the board is not covered by warranty. **To avoid overheating, the board must be installed in a well-cooled workstation, server or industrial chassis PC**. Installation in a PC or workstation without **fans at the front end of the card cage will cause the board to overheat, and resulting damage is not covered by warranty. If after 5 minutes of operation the heatsink on the board feels too hot to comfortably touch, a system with better cooling is required**.

1. Use the shutdown command, turn off the system power, and disconnect the power cord.

BEFORE REMOVING THE COMPUTER SYSTEM COVER OR REMOVING ANY BOARD, BE SURE THAT THE POWER TO THE COMPUTER, AS WELL AS TO ALL PERIPHERAL DEVICES IS OFF. WEAR A STATIC-DISSIPATING WRISTBAND WHICH IS GROUNDED TO THE SYSTEM CHASSIS WHILE OPENING OR WORKING ON YOUR SYSTEM.

2. Remove any screws that attach the computer system cover and remove the cover.

3. Remove the filler bracket from the PCIe slots the board will occupy **and the filler bracket from the PCIe slot below the board, to allow adequate air flow across the board's heatsink**.

4. Hold the board by the top of the metal bracket and the back of the board (**Do NOT EVER hold or exert any force on the DIMM memory modules**). Carefully slide the board in so its PCIe connector mates with the motherboard PCIe connector. **Do not force the board. If there is any resistance, rock the board slightly when inserting it.** Be sure the board is seated firmly into the motherboard PCIe connector. Check that no other PCIe/PCI boards have become unseated.

5. Plug coaxial I/O cables for the analog inputs and/or outputs into the appropriate SMA connectors on the board. Connect the free ends of the analog input cable to the signal sources to be digitized, and connect the clock input cable to a suitable clock source, if using an external clock.

6. Replace the computer system cover, installing all screws you removed. Reconnect the power cables to the system and peripherals. Power up and reboot the system. The system will then be ready for software installation.

In some systems the configuration time of the on-board FPGA may be long enough that the FPGA is not fully configured before the system begins accessing the board. If the board is not recognized by the system (e.g. not present in the Device Manager (Windows) or not shown using lspci (Linux)), or the system hangs when accessing the board or other similar errors occur then this may be the problem. This is particularly possible with board models using the denser FPGAs, such as the XC5VLX155T, but is still rarely a problem. If any of these issues are seen the system will need to be "warm restarted" before the board can be used. The easiest way to do this is to boot the system to the OS boot menu, then restart the system without powering it off, then let the system start normally. This allows the FPGA sufficient time to fully configure (a result of powering on) before it is assessed. This can be easily done by adding a "reboot" option to the GRUB boot loader in Linux, hitting this reboot option after the first cold boot, and then allowing the system to continue to reboot again with its normal default boot option.

13. Software Installation and Setup

"Newer boards may have FPGA firmware that is different from earlier firmware versions shipped with prior boards of this model. To ensure correct operation of your new board, **please download the current software package from Ultraview's website. Do not install older versions of drivers or user software that you may have used with previously purchased boards. You may also need to recompile custom user software you may have written**, so it will correctly run with the current driver and board firmware."

For users who modified a previously LabVIEW™ release and wish to update their projects to work with the latest software, see "APPENDEX – How to Update Your LabVIEW™ Project".

13.1 Software Installation for Windows 7, 8, Vista™, and XP™

The Windows software release can be downloaded from the following URL:

http://www.ultraviewcorp.com/downloads

To install the software place the Windows release into a directory on your local drive. Please quickly read the README file provided in the root of the release for an understanding of the files provided.

To run the LabVIEW executables, the LabVIEW Run-Time Engine 2012 (32/64-bit) should be installed.

Windows should prompt with its standard "New Hardware Found" or equivalent dialog box. Select "Install hardware from known location" (or equivalent) option, this is usually the second of two options (the first being to install automatically). In the dialog box which follows, please include in the search location the directory the release files were copied to. Note that Windows will search for the file AD83000x*.inf, which must be in the directory specified to be included in the search. After successful installation, the device driver will have successfully attached to the device. After installing the driver, a system reboot may be necessary.

To avoid data overruns, interruptions in data acquisition, and hanging of user programs, **turn off all system power management options, screen savers, etc. The system must not be allowed to go into sleep mode when the board is running.** To run the example programs for Vista or XP, go to the section below, "Running the Example Programs under Windows Vista or XP™"

13.2 Software Installation for Linux (64-bit)

Centos 6.2 is the only currently supported Linux operating system.

To avoid data overruns, interruptions in acquisition, and hanging of user programs, **turn off all system power management options, screen savers, etc. The system must not be allowed to go into sleep mode when the board is running.** Also the system must have at least 2GB of installed RAM to acquire data records in the multi-hundred megabyte size, at full speed, unless a suitably fast hardware RAID system is present.

After installing the board, insert the installation diskette and log in as **root**, copy the file **uvdma-x-**

y.z.x86_64.rpm to any directory (x,y,z are integers denoting the current revision of the Linux release, below the revision is shown as 1-1.10), and type in the following line at the prompt (shown here as #):

rpm –ivh uvdma-1-1.10.x86_64.rpm

The installation script will automatically create a directory /uvdma, and install the software in this directory. Precompiled driver modules are supplied and must be loaded as follows:

cd /uvdma/driver/src
rmmod uvdma
insmod uvdma.ko

To uninstall the RPM, as required prior to installing a newer version of software, the following command is used:

rpm –e uvdma

To insure correct operation of the device driver with your kernel version you may be required to recompile the driver module. Before recompiling the driver module a link to the kernel source must be setup. Ensure that the gcc package is installed by running "yum install gcc". The driver module can now be built, **you must then reboot** before going further.

14. Running the Example Programs

The software provided allows the A/D boards to be run under either a Command Prompt under both Windows and Linux, as well as in LabVIEW for Windows.

See Section 13.2 for how to run the LabVIEW project.

See Section 13.3 and 13.4 for how to run the Command Prompt project

14.1 Preparing to Run/Modify the Example Programs

The software release has both source and executables for the various example programs, which can immediately be run to demonstrate the use of the board, and form an excellent basis for developing your own custom software. The source code for both the command line Linux example programs and the command line Windows example programs share an identical section of cross platform source code; this common section of code, located in directories “AppSource” and “_DllSource” in the release, and can be compiled under Linux or Windows.

Usage information for the applications is available by simply running the executable without any arguments. The file "ultra_config.dat" contains calibration settings (offset/gain) of each board based on serial number, if the user would like to change these modify this file. Additionally, “ultra_config.dat” contains information which tells the user applications information regarding the board according to the board's serial number.

For Linux:

The example programs can be rebuilt under Linux by typing “**make**” from “/uvdma/example_programs/_DllSource” and “/uvdma/example_programs”. Typing “**make clean**” clears all executables so that “make” can write new files. The gcc-c++ package must be installed; under CentOS, the command "yum install gcc-c++" will install gcc-c++. Visual Studio

project files are also provided for all sample user programs under Windows Windows, allowing for easy modification and recompilation.

For Windows:

For users who modified a previously LabVIEW™ release and wish to update their projects to work with the latest software, see “APPENDEX – How to Update Your LabVIEW™ Project”.

The DLL/Acquire program were compiled using Microsoft Visual Studios 2010 Ultimate.

The LabVIEW project was developed with LabVIEW 2012 32/64-bit Professional Development System.

To recompile the DLL:

1) Open "PCIeDAQ_Windows_All_X-Y.Z_TTUUVV-W_BUILD_1MB_QQBITDLL/_DllAndTestProjects/Project AcqSynth/**AcqSynth.sln**"

2) In the "Build" tab, select "Rebuild Solution"

To recompile the Acquire program:

1) Open "PCIeDAQ_Windows_All_2-0.11_052913-1_BUILD_1MB_64BITDLL/Project Acquire/**acquire.sln**"

2) In the "Build" tab, select "Rebuild Solution"

Do not open any “.vcproj” as they are not updated and point to old directories. The quickest way to undo is to unzip a new folder and open the “.sln” files.

The resulting executables are built into the “build” directory in the Windows release.

Note: Rare occasions Linux machines do not recognize the driver automatically. To resolve, in a command prompt:

 # dmesg | grep uvdma

Example output after “dmesg | grep uvdma:

```
uvdma_init(): as root, manually run cmd: mknod /dev/uvdma0 c 249 0
uvdma_pci_probe(): v_june2_2012, devices found 0
uvdma 0000:01:00.0: PCI INT A -> GSI 16 (level, low) -> IRQ 16
uvdma_pci_probe(): detected Ultraview PCIe board pci_devp=0xffff88021a1c1000
uvdma_pci_probe(): resetting DDR firmware
uvdma_pci_probe(): unresetting DDR firmware
uvdma_pci_probe(): board 1  assigned IRQ=16
IRQ 16/uvdma-ad83000: IRQF_DISABLED is not guaranteed on shared IRQs
uvdma_interrupt_handler(): ISR num_adc_ints set to 1 !
uvdma_pci_probe(): 64 bit DMA OK
uvdma_pci_probe(): allocated page table array at 0xffff880218d00000
uvdma_pci_probe(): Enabling Interrupts
uvdma_init(): register driver 0
```

Follow the uvdma_init() line and type:

 # mknod /dev/uvdma0 c 249 0
 # chmod a+rwx /dev/uvdma0

Now the software should be ready to use.

14.2 LabVIEW™ The Graphical Waveform Viewer under Windows 7™, Vista™ or XP™

The LabVIEW project incorporates all of the same features as the 'acquire.exe' command but has the advantage of displaying the data acquired. To run the LabVIEW executables, the user must first download the LabVIEW 20XX 32/64-bit Run-Time Engine, depending on the description of the software package.

Quick Start in Continuous:

1) In the "build" directory, double-click either **LabVIEW_Acquire_Data_x64.exe** or **LabVIEW_Acquire_Data_x86.bat** depending on the system OS.
2) In **ReadGraph.exe**, press **Run/Stop** under the **Continuous** tab.
3) At this point, the board should be running in Continuous mode using the internal clock with no triggering. Data is simply being read from the board and is **NOT being stored to disc.**

Quick Start in Acquire Once:

1) In the "build" directory, double-click either **LabVIEW_Acquire_Data_x64.exe** or **LabVIEW_Acquire_Data_x86.bat** depending on the system OS.
2) In **ReadGraph.exe**, select the **Acquire Once** tab, and press **Acquire.**

   At this point, the board should be running in Acquire Once mode using the internal clock with no triggering. Data is simply being read from the board and **IS being stored to disc** in the "build" directory with the file name **uvdma.dat** with a size of **1MB** when the **# of Blocks to Acquire** is "1".

The board comes with a powerful LabVIEW™ based graphics program for Windows, **SetupControlv2.exe** and **ReadGraph.exe**, located in the build directory of the PCIeDAQ folder. This GUI allows acquisition and display of data from any Ultraview PCIe board.

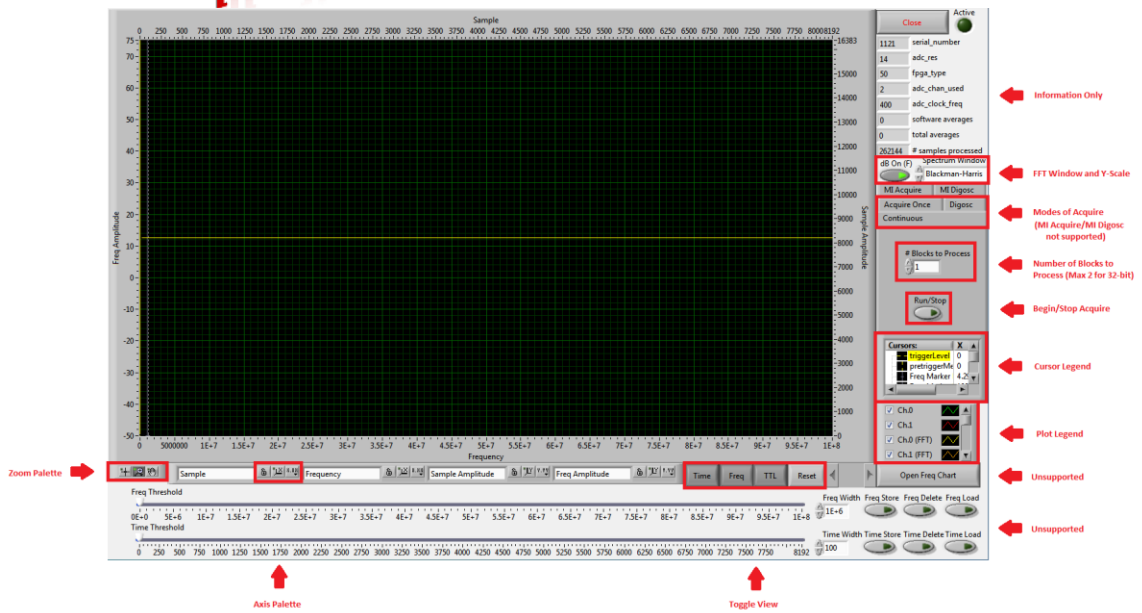


Figure 13.2.1 ReadGraph.exe

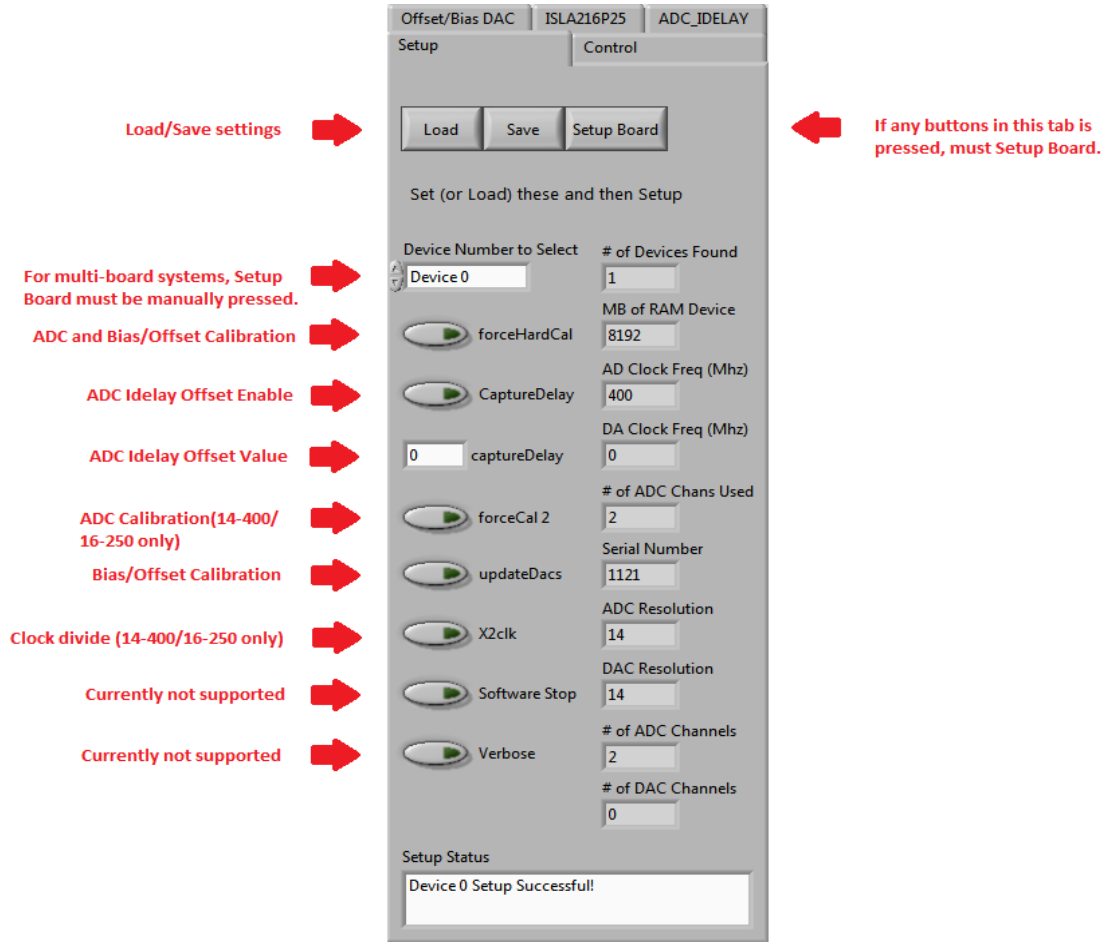


Figure 13.2.2 SetupControlv2.exe

The two executables communicate over TCP/IP to share important board configurations.

ReadGraph acts as the client, and SetupControlv2 acts as the server. For the user's convenience, **LabVIEW_Acquire_data_x64.**exe and **LabVIEW_Acquire_Data_x86.bat** are simple batch files to open both programs so that TCP/IP connects properly. To do this manually, the user must open SetupControlv2.exe FIRST and ReadGraph.exe SECOND. Do not try to Run the board before first pressing “Select Device” and “Setup Board”.

When running **SetupControlv2**, the first tab displayed in the program is the "**Setup**" tab. Use the "**Load**" button to load the device and configuration settings from the previous running of the program. Modify these settings and press the "**Save**" button to save configuration settings. Next, change **“Device Number to Select”** (starting at 0) and click **“Select Device”** to place a handle on the board. **Note: These configuration settings are the same as used for the acquire program. Triggering and select recording options are explained in Section 13.4.1.** Having set the configuration values for your type of acquisition, use the “**Setup Board**” button to configure the device before acquisition. After board setup has completed successfully, the “Control” tab has additional features that can be configured post-setup even while the board is running.

Note: The board has not yet begun acquiring.

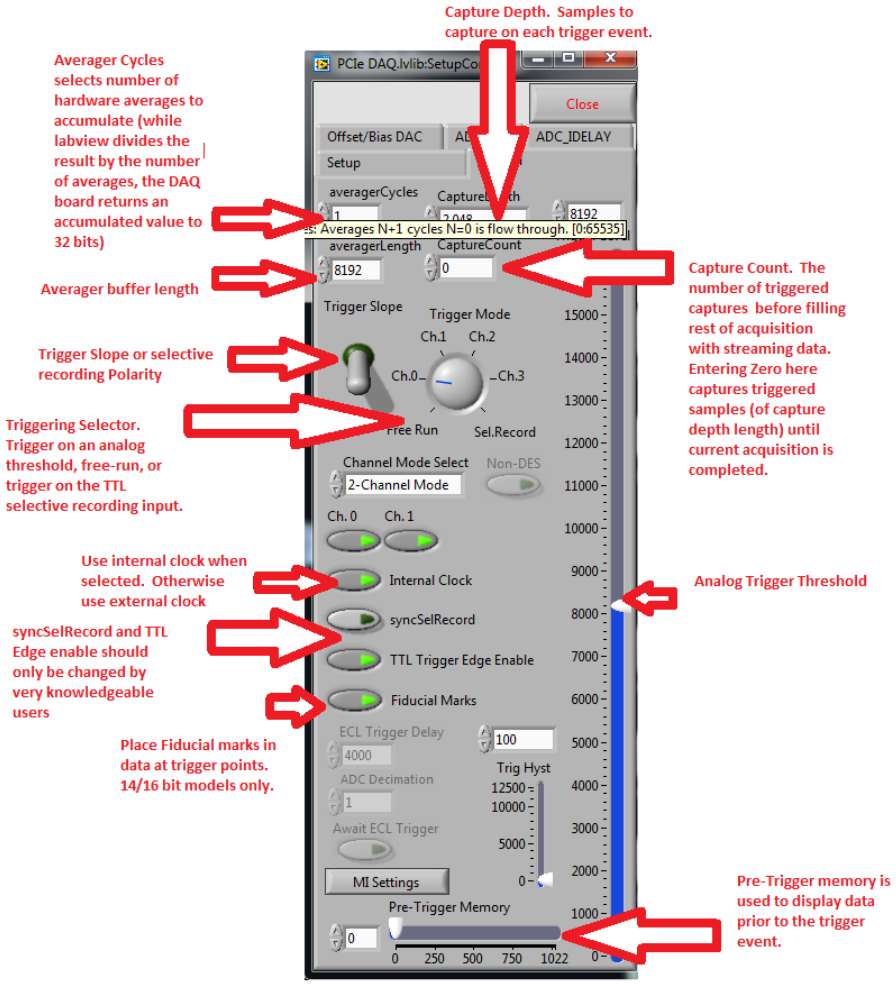


Figure 13.2.3 Control tab in SetupControlv2.exe

The "**Trigger Mode**" selects which input to trigger from. **"Free Run"** is normal acquisition with no triggering. "**Ch.0**", "**Ch.1**", "**Ch.2**", and "**Ch.3**" are all the analog waveform triggers which use **"Trigger Level"**, **"Trig Hyst",** and **"Trigger Slope"** to determine where a valid trigger occurs on the waveform. When triggering on an analog waveform, "**TTL Trigger Edge Enable"** needs to be on. **"Sel.Recording"** mode is selective recording using the Acquire Disable In or Sync/Selective Recording In Jack. **"syncSelRecord"** can be used with the **"Sel.Recording"** as described in Section 13.4.1. **"Heterodyne"** mode is used with the heterodyne triggering described in Section 2.5 and 2.6 for AD14-500x2 and AD16-250x2/x4 boards, and the Heterodyne Trigger In Jack. Keep in mind that **"Trigger Slope"** needs to be low for normal acquisition as it is associated with the selective recording polarity.

For all triggered modes of acquisition the AD14-400x2 adds programmable capture length. For each recognized trigger (TTL edge or analog threshold), the board will acquire "Capture Depth" number of samples. Note that if "Capture Depth" is zero then once triggered the data will be recorded until the acquisition is complete (normal mode). There is an added "Capture Count" modifier, which programs how many trigger events to record before resuming normal capture operation. Since our minimum block size to acquire is 1Mb, and a user may have a situation where only a limited number of triggers are going to be produced, using the "Capture Count" flushes out the rest of the buffer after a programmed number of triggers.

Note: For Analog Waveform Triggering and Heterodyne Triggering, TTL Trigger Enable must be on.

"Offset/Bias DAC", "ISLA21P25", and "CE/RST/INC" tabs are for calibration and debug use only.

When running **ReadGraph**, the time and frequency graphs are **overlayed** onto a single graph. The **left and bottom axes** are for the **frequency domain response**, while the **top and right axes** are for the **time domain response**. Simple **"Time"** and **"Freq"** buttons are available to easily hide Time or Frequency Plots. The **"Reset"** button resets the X and Y scales to default values. There are three tabs on the right which control what to display on the graph: "**Continuous**", "**Acquire Once**", and "**Digosc**".

MI Acquire and **MI Digosc** are for internal use only.

In the "**Continuous**" mode, use the "**Run/Stop**" button to start and stop acquisition of data. In this mode the board is used to acquire and display a very small amount of data. In this mode, the board starts acquisition. After accumulating the desired number of blocks, the data is displayed. The board starts again, and this cycle repeats as long as the "Run/Stop" button is pressed. This mode is useful for quick observation/verification of real-time data. When triggering, convenient cursors are shown to indicate the waveform trigger threshold and pre-trigger value. Additional cursors can be made and customized by right-clicking the cursor legend. In the Continuous tab, the user can adjust the number of 1MB blocks for LabVIEW™ to process by increasing the "**# Blocks to Process**". The Continuous mode sets the board up to acquire 1 or 2 blocks at a time, and **does not store data to disk!**

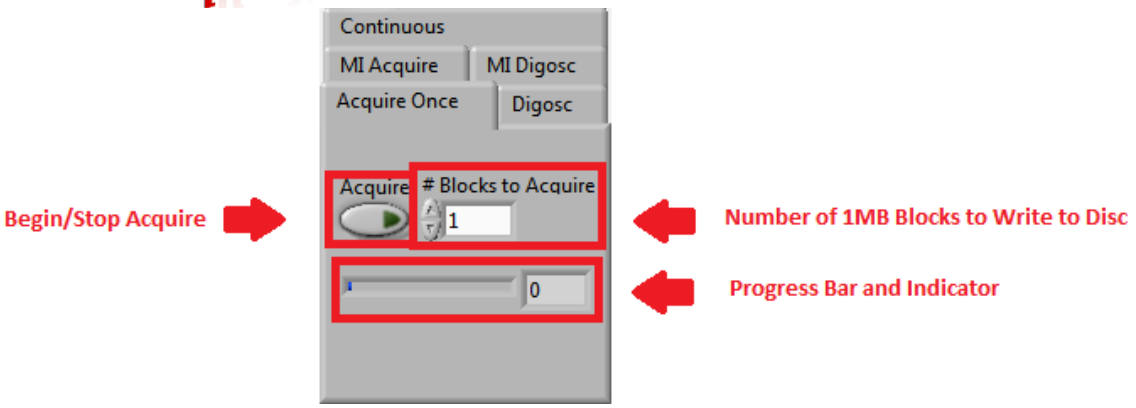


Figure 13.2.4 Acquire Once tab

The "**Acquire Once**" tab can be used to acquire the previously specified number of 1MB blocks of data to a file and then view the data. Specify the number of blocks to acquire by changing the "# **Blocks to Acquire**" before pressing "Acquire". When using Acquire Once, the user can specify 8192 blocks guaranteed without overruns and data is stored to "uvdma.dat". **Specifying more than 8192 blocks may result in overruns if the external clock is too fast.** When the Acquire button is pressed, each 1MB of data is displayed and stored in uvdma.dat in the build directory.

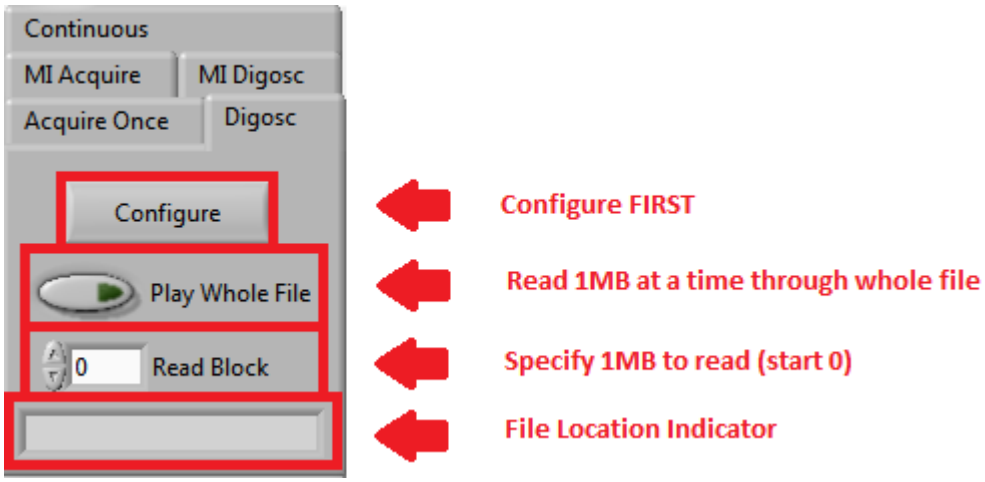


Figure 13.2.5 Digosc tab

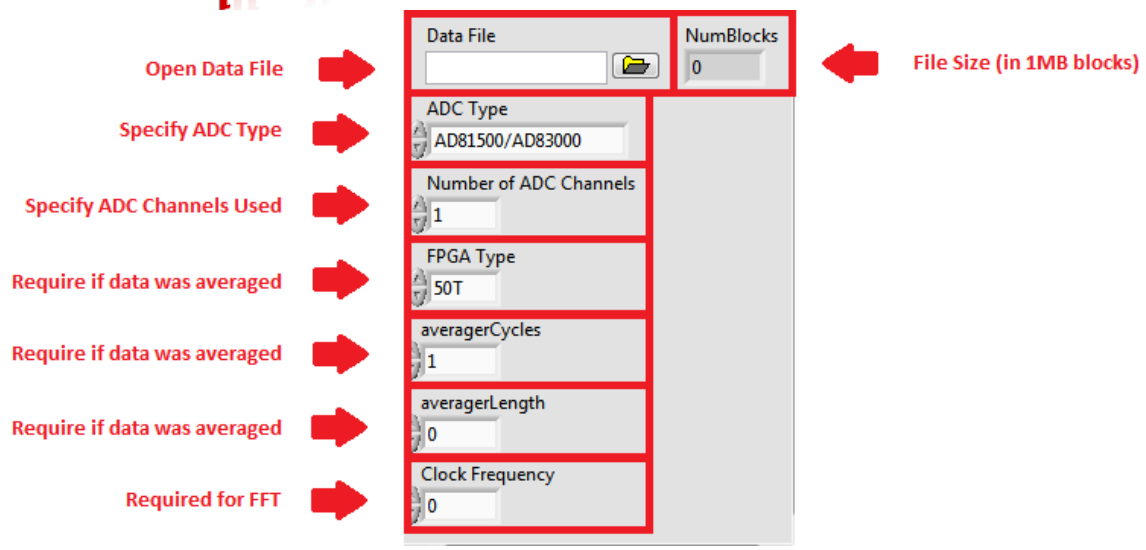
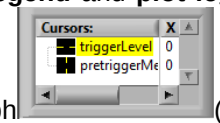
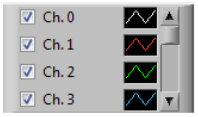


Figure 13.2.6 Configure tab

The "**Digosc**" tab can be used to display previously acquired "uvdma.dat" files in the time domain. In the "Digosc" tab, press the **"Configure"** button to open the settings window. Open the **"Data File"**, specify the **"Number of ADC Channels Used"**, **"FGPA Type"**, **"averagerCycles"** (1 = no averaging), **"averagerLength"**, and **"Clock Frequency"**. **"Play Whole File"** will read each block until the end of file. Change **"ReadBlock"** to read a specific block in the file.

Built-in LabVIEW™ panning and zoom utilities are available on the **bottom and bottom-left** of the graph  (zoom palette)  (axes palette). Right-clicking the graph itself allows for more graph options. **Built-in LabVIEW™ cursor legend** and **plot legend** are made available to the user on the **bottom-right** of the graph  (cursor legend)  (plot legend).

Note: There is a LabVIEW™ bug where the checkbox for the first channel does not work. Instead, left-click on the plot icon and deselect "Plot Visible".
Note: There is a LabVIEW™ bug where the plot legend retains all plots in the list, even if there is no data in those channels. So ignore the long list.

At any time the user wishes to return to default window settings, the "**Reset Graph"** will do just that.

In all modes of the LabVIEW™ project, the "Num Blocks to Process" should never be greater than the "Number of Blocks to Acquire".

For AD14-400 boards shipped prior to 2/26/13, users will have to "SetupBoard" if any controls are changed in SetupControlv2 OR upgraded firmware to the latest. Please inquire on upgrade procedure.

To properly close the LabVIEW software without any warnings popping up about TCP/IP error, close SetupControlv2.exe FIRST, then close ReadGraph.exe SECOND.

14.3 The Graphical Waveform Viewer under Linux

The application “digosc” displays, in waveform format, the A/D data acquired by the board. This graphical waveform viewer can be used to read data from a previously stored record on the hard disk. For usage of digosc perform the following commands and read all statements printed, further details can be found in the comments in digosc_3000.c.

cd /uvdma/example_programs
./digosc

The program will display a blank screen while reading data from the file. To display the contents of any desired block type the block number into the text field and then click “Update”. The scroll bar then allows any portion of the block to be displayed; note that the number displayed on *the scroll bar* indicates the offset in the block of the first sample plotted on the screen. To display a different block, hit the up arrow (or type in the new desired block number) and click the “Update” button. **The data shown is not valid until “Update” has been pressed, the "Update" button must be pressed after the program first runs for even the very first data to be accurate**. Then, you may scroll through the new block using the scroll bar.

This example program may be recompiled by typing “make all” or “make digosc”. This program requires the GTK2 libraries to be installed, running "yum install gtk2-devel" will install the GTK2 packages.

14.4 Cross Platform Command Line Acquisition & Synthesis

Both the Windows and Linux software releases include the same C source code files that implement a program to acquire data to disk and a program to synthesize data from disk. The Windows release includes these files as Visual Studio projects and the Linux release includes these files in /uvdma/example_programs/AppSource and /uvdma/example_programs/_DllSource, each with an included makefile.

The example programs, which can be run to demonstrate the use of the board, are also an excellent (and the only supported) means for developing custom software. Full source and a makefile are provided for all sample user programs (in the subdirectory example_programs), allowing for easy modification and recompilation.

14.4.1 acquire - acquire data into on-board DRAM, and then store the buffer to disk.

The program acquire acquires a selectable number of DMA blocks of data into the board's onboard memory and then move the data to a file on disk.
The program acquire can be used to acquire data to the board’s on-board RAM, followed by an automatic storage of the board’s buffer to a disk file. **For usage of acquire, perform the following commands and read all statements printed, further details can be found in the comments in acquire.c.** A minimum of 1 1MB blocks of data can be acquired, there is no maximum.

cd /uvdma/example_programs
./**acquire**

Ex. ./acquire //Linux
acquire //Windows

// This will prompt a list of options the user can use to configure the board when acquiring

Ex. ./acquire 1 –ic //Linux
// acquires 1MB using internal clock with no triggering and stores to disc in the build directory with file name uvdma.dat

Note: In Windows, the acquire program is accessed through the "Command Prompt" in the "build" directory. Simply type "acquire" in the Command Prompt for a list of operations.

Ex. acquire 1 //Windows
// acquire 1MB using external clock with no triggering and stores to disc in the build directory with file name uvdma.dat

The acquire program has several different modes of operation. In the simplest case, the board acquires to onboard DRAM while continuously reading from the board into a small bounce buffer allocated in host memory and then writing from the bounce buffer to disk. In this case the board can acquire up to the size of the board's memory without any limitation on incoming data rate, or for a very long time if the disk DMA rate is sufficient relative to the incoming date rate. Alternatively, the acquire program can be compiled to use a large amount of system memory (typically limited to the amount of system memory minus a couple gigabytes) to increase the capture length. In this case writing to disk is delayed until the capture is completed, data is acquired into onboard DRAM and DMA'ed to the allocated system memory until this system memory is filled then the board's memory is filled until it contains only new data (data not yet transfered to the host). In this case the acquisition rate is limited to approximately the DMA rate of the system.

The acquire program offers both triggering and, on 14-bit and 16-bit models, selective recording. The board defaults to active LOW, selective recording. For example, if the board is prepared such that there is no trigger signal connected to the "Acquire Disable (Trigger)" SMA jack with the command "acquire 1 -ic", the board will continuously acquire. However with the same command, if the board has the proper trigger input (see board specifications under "Optional (Selective Recording) Input)", the board will disable acquisition when the trigger signal is HIGH and will enable acquisition when the trigger signal is LOW.

Special arguments for AD8-3000, AD8-1500, and AD12-1800 boards:

1) "-ecltrig" Waits for ECL trigger from the Trigger Sync SMA Jack on the 8-bit RevD boards or similarly the Sync A/D SMA Jack on the 9-bit RevB and RevC boards.
2) "-ecldelay" Sets the ECL trigger delay.

64us * (1clk cycle)/(8 samples) * clk_rate (samples /s)

Example: clk_rate = 1GHz => ecldelay = 8000

Default: ecldelay = 8000

Special arguments for AD14-400 (boards after 6/24/2013):

1) “-capture_depth” <n>. Captures <n> samples for every trigger (only applies to triggered modes) . Defaults to zero, which is normal triggered capture till acquisition complete.
2) “-capture_count” <n>. Captures <n> trigger events of “capture_depth” samples, Followed by continuous capture until acquisition is complete. Only applies if (capture_depth > 0) Defaults to zero, which is triggered captures of capture _depth number of samples until acquisition is completed.

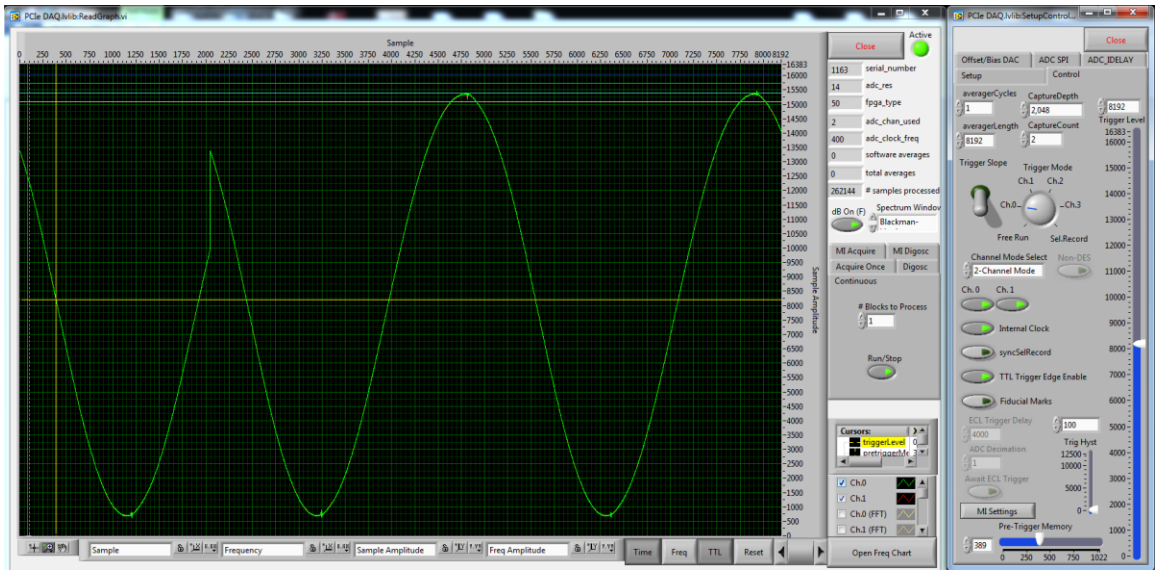


Figure 13.4.1 Shows capture_count = 2, capture_depth = 2048. The triggers start at 0 and 2048, data is captured continuously after the second trigger.

Special arguments for AD14-400 (boards after 2/26/2013), AD14-500 and AD16-250 boards:

1) “-syncSelRecord” Waits to record until the “Acquire Disable” input transitions from “disabled” to “enabled. For example the command : “acquire 1 –syncSelRecord” will wait until the selective recording input transitions from High to Low Low to begin recording. Whereas the command: “acquire 1 –syncSelRecord -ttlinv” will wait until the selective recording input transitions from High to Low to begin recording. This enables the user to be certain of the timing of the first block of data relative to the “Acquire Disable” input. The recorded data is shifted by 13 samples relative to the “Acquire Disable” input, such that there are 13 samples of pre-trigger memory. The user should be aware that this also means that when “Acquire Disable” goes to disabled, the last 13 samples are not recorded.

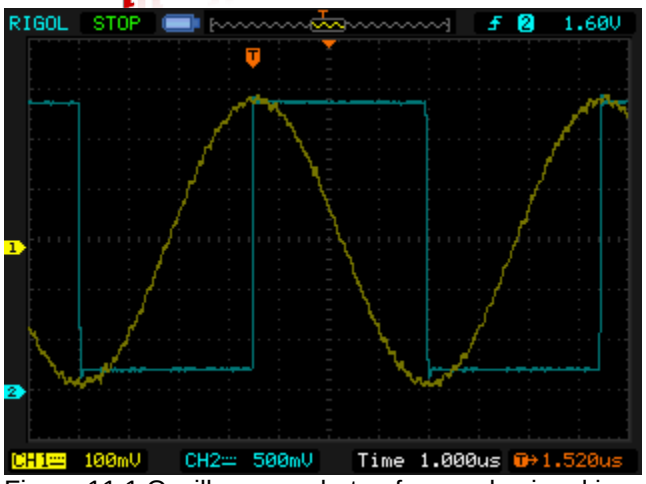


Figure 11.1 Oscilloscope photo of example signal input (yellow) and Acquire Disable input (blue) to the AD16-250.

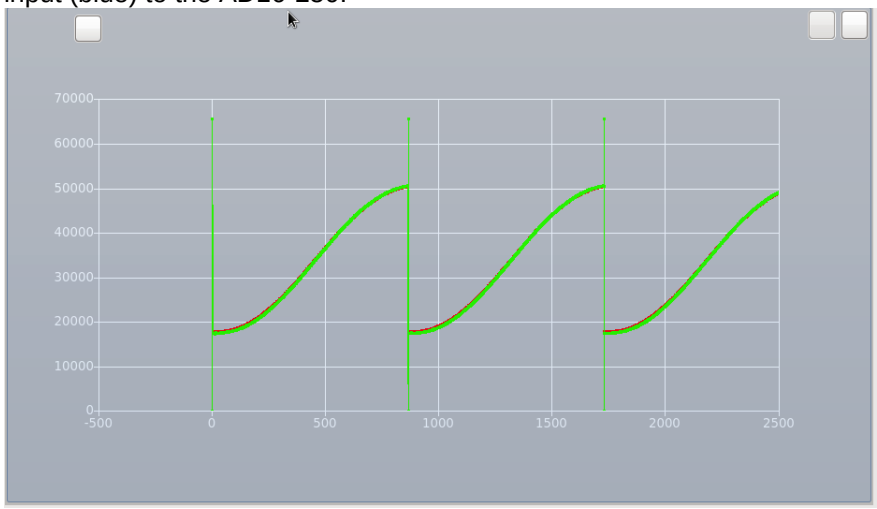


Figure 11.2 Plot showing data captured as in 11.1 using the command:
./acquire 1 –ic –syncSelRecord –fiducial

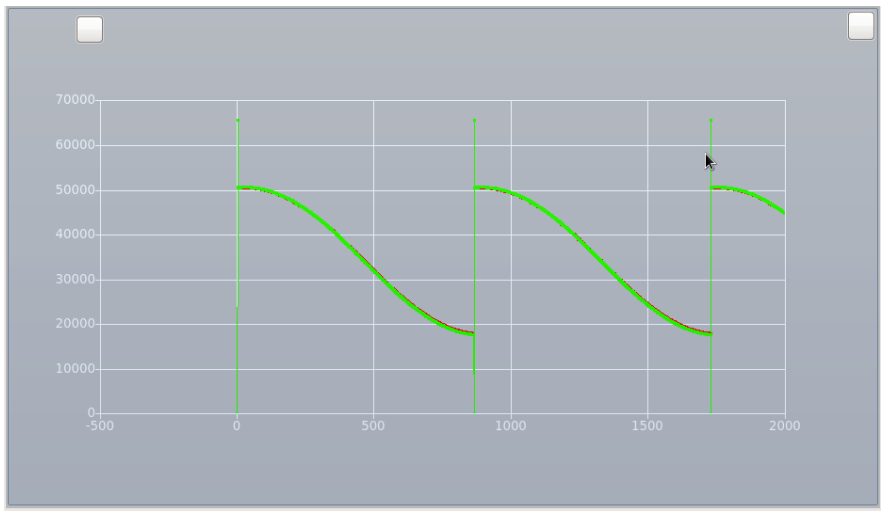


Figure 11.3 Plot showing data captured as in 11.1 using the command:
./acquire 1 –ic –syncSelRecord –fiducial –ttlinv

2) “-fiducial” places fiducial marks at the beginning of each selective recording. Fiducial marks are as follows:

a. 1 channel mode: chA 0x0000 , 0x0001, 0xFFFF, 0xFFFE, 9 pre-trigger samples, Aligned data.
b. 2 channel mode: chA 0x0000, 0xFFFF, 11 pre-trigger samples, Aligned data. chB 0x0001, 0xFFFE, 11 pre-trigger samples, Aligned data.

3) “-X2clk” sends a SPI command to the ADC to operate at ½ the supplied clock

4) “-cal” writes the SPI command to the ADCs’ gains and offsets.

5) “-averager <N>” enables averaging of the waveform where N = [0,65535] (0 = no averaging).

a. When averaging 1 channel of data, the averaging buffer size is 16383 samples.
b. When averaging 2 channels of data, the averaging buffer size is 8192 samples.
c. When averaging 4 channels of data, the averaging buffer size is 4096 samples.

The averager waits for a valid trigger to occur (analog waveform, TTL, or heterodyne). Once a valid trigger is found, the average collects the averaging buffer size worth of data, holds it in memory, and evaluates whether it has accumulated enough times (N times). If it has not accumulated enough times, it will wait for the next valid trigger and add it into its previous stored data. Once it has accumulated enough data, it will start the next buffer. This process will repeat until all requested blocks of data has been acquired

6) “-trigger_en” allows for analog waveform triggering. (Default falling edge)

“-ttlinv” for rising edge trigger

7) “-trigger_ch (Chan N)” to select which channel to analog trigger from. (Chan N) must be either 0,1,2, or 3.

8) “-thresh_a <N>” for analog trigger threshold. N=[0,65535]

9) “-thresh_b <N>” for analog trigger hysteresis. N=[0,65535]

thresh_b should always be greater than thresh_a whether rising edge or falling edge.

10) “-pretrigger <N>” for pretrigger memory after trigger is acquired. N=[0,511].

Appending **“-ttlinv”** to the original acquire command will modify the trigger condition to an active high. For example, “acquire 1 -ic -ttlinv” will acquire 1 blocks with the internal 400MHz clock only when the selective recording trigger signal is HIGH.

Triggering allows for continuous acquisition, beginning at the first rising or falling edge (depending if “-ttlinv” has been asserted) of the trigger signal and stopping only when all data has been acquired. To assert triggering, append **“-ttledge”** to the command line. For example, “acquire 1 -ic -ttledge” will acquire 1 blocks with the internal 400MHz clock and edge triggering.

To use an external clock instead of the internal clock, simply leave out **“-ic”** in the command. For example, “acquire 1” will acquire 1 blocks with an external clock and

active low, select recording. When using the internal clock, the external clock SMA must remain unconnected.

For multiple channel boards, the **"-scm"** extension enables single-channel mode. When using this option, also use **"-scs"** to specify which channel to acquire from (single-channel select) starting from "0". For the channel not used, make sure to leave the input unconnected. For boards with four channels, the **"-dcm"** extension enables dual-channel mode, and **"-dcs"** is used to specify which two channels to acquire from (dual-channel select). Valid entries for "-dcs" are "01"/"10" for channel 0 and channel 1, "02"/"20" for channel 0 and channel 2, "03"/"30" for channel 0 and channel 3, "12"/"21" for channel 1 and channel 2, "13"/"31" for channel 1 and channel 3, and "23"/"32" for channel 2 and channel 3. For example, "acquire 1 –ic –dcm –dcs 10 will acquire 1MB of data from channel 0 and channel 1 using the internal clock. Data will output the first sample of channel 0 first, then channel 1 regardless when specifying "10" or "01".

Note: Both triggering and selective recording use the "Acquire Disable (Trigger)" SMA jack as its input. Only 12, 14 and 16 bit boards have selective recording. On 8 bit boards, edge triggering must be a rising edge and is not programmable.

Multiple boards can be armed to acquire data in response to the same external trigger by arming them using multiple instances of the acquire program. Run the acquire program with no options and view the output for usage on how to select which board is targeted when running the program. To target a specific board, append the extension **"-b 0"** to target device 0, and **"-b 1"** to target device 1. **Device 0 will output data into udvma.dat, while device 1 will output data into uvdma1.dat, and so on.** In LabVIEW™, multiple boards will not automatically set. So the user will need to "SetupBoard" for the selected device prior to acquiring data.

14.5 Cross Platform Command Line Options

acquire (N blocks) [OPTIONS]

Acquires specified number of blocks. Number of blocks option must always be first.

The following [OPTIONS] may follow the number of blocks option in any order:

For all boards:

"-ic" Board will use the internal clock, do not connect an external clock. If not specified board uses external clock.

"-scm" Run multi-channel boards in single channel mode. Not required for single channel boards.

"-scs (Chan N)" When running multi-channel boards in single channel mode use\n\t\tchannel (Chan N).

"-dcm" Run multi-channel boards in dual channel mode. Not required for dual channel boards.

"-dcs (Chan NM)" When running multi-channel boards in dual channel mode. (Chan N) must be either 01,10,02,20,03,30,13,31,23, or 32. "-dcm" must be asserted.

"-b (BoardNum)" Acquires from the specified board. Do not specify the same board from two separate consoles. BoardNum starts at 0.

"-t" Run a DMA throughput test for the specified number of blocks. (unsupported)

"-ttlinv" Inverts the TTL trigger. Default is active low TTL trigger.

"-user (value)" Specifies a user value to configure ADC processing. (unsupported)

"-capture_depth <N>" Fixed sample-size capture after each trigger. Sizes are in exact multiples of 8 up to 2^32 samples. Must be used with valid triggers. N=0 is normal acquisition. Default N=0.

"-capture_count <N>" Specifies the number of triggers to acquire with size capture_depth. N=0 is infinite triggers until desired number of blocks is acquired. Default N=0.

"-v" Enable extra print statements.

For AD8-1500, AD8-3000, AD12-1800:

"-ecltrig" Sets acquisition to await ECL trigger.

"-ecldelay" Set the ECL trigger delay. Default = 4000. See manual for details.

"-dec (factor)" Enables input sample decimation. (factor) can be 1,2,4,8 or 16. Up to x16 on AD8-3000/AD8-1500. Up to x8 on AD12-1800.

For AD12-1800:

“-desiq” Sets the AD12-1800 to DESIQ single channel mode. Both inputs must be externally driven. In DESIQ, the I- and Q- inputs are shorted together. “-scm” must be asserted.

“desclkiq” Sets the AD12-1800 to DESCLKIQ single channel mode. Both inputs must be externally driven. In DESIQ, the I- and Q- inputs remain electrically separate, increasing input bandwidth. “-scm” must be asserted.

For AD14-400, AD14-500, AD16-250:

"-ttledge” Sets acquisition to await TTL trigger edge.

"-cal” Update ADC registers from config file

"-dacs” Write offset and bias DACs.

"-X2clk” ADC operates at 1/2 supplied clock

"-hardcal” Forces calibration

"-fiducial” Places Fiducial marks in data when trig/sel record starts recording

"-syncSelRecord” Waits for trig/sel = FALSE (follows ttlinv) to arm selective recording

"-capturedelay N” (delay N=0-63) Overrides adc clock to data capture delay (14 bit boards only)

"-averager <N>“ (N=0-65535)\tAverages N+1 cycles, N=0 is flow through mode

"-averager_len <N>”

For 50T:
1-channel mode: N=16384(Default),8192,4096,2048,1024,512,256,128,64,32,16
2-channel mode: N=8192(Default),4096,2048,1024,512,256,128,64,32,16,8
4-channel mode: N=4096(Default),2048,1024,512,256,128,64,32,16,8,4
For 155T:
1-channel mode:
N=131072(Default),65536,32768,16384,8192,4096,2048,1024,512,256,128,64,32,16
2-channel mode:
N=65536(Default),32768,16384,8192,4096,2048,1024,512,256,128,64,32,16,8
4-channel mode:
N=32768(Default),16384,8192,4096,2048,1024,512,256,128,64,32,16,8,4

"-trigger_en” for analog waveform trigger. Use -ttlinv to specify rising or falling edge.

"-pretrigger” for pretrigger memory after trigger is acquired. pretrigger must be 0 to 512

"-trigger_ch (Chan N)” for analog waveform trigger Used with -ttledge and -averager. Must be either 0,1,2, or 3.

"-thresh_a <N>” for analog waveform trigger threshold. <N> = [0,65535].

"-thresh_b <N>” for analog waveform trigger hysteresis. <N> = [0,65535].

"-clock_sleep”

For AD14-500, AD16-250:

"-heteroDiode" for heterodyne triggering.

15. TTL Input Panel for AD14-400x2 and AD14-500x2 models

Models AD14-400x2 and AD14-500x2 allow concurrent high speed acquisition of up to Four TTL signals, at the same rate as, and time aligned with, the A/D sampling. This feature is useful for correlation of analog/RF signals and the TTL control signals in the system. For example, a rotating RADAR antenna's position may be monitored using the TTL inputs, while the received RF signal is concurrently acquired by the two high-bandwidth analog inputs. These TTL bits are easily inputted to the AD14 board via the small TTL boardlet and uDB26 cable provided with these boards. One end of the cable should be connected to the installed data acquisition card, and the other end should be connected to the TTL boardlet shown below.

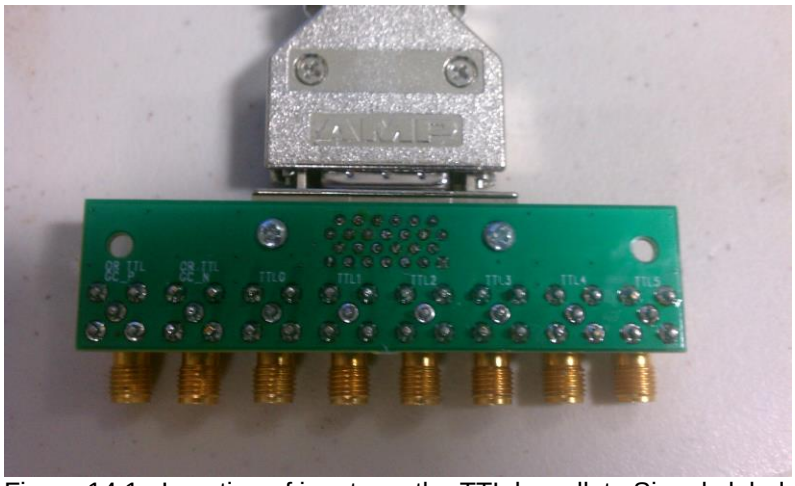


Figure 14.1. Location of inputs on the TTL boardlet. Signals labeled TTL0, TTL1, TTL2 and TTL3 are the four TTL bits that are acquired synchronously with the A/D data and are stored in the two most significant bits in each 16-bit sample word. TTL4, TTL5, GC_P, and GC_N are reserved for OEM use and are normally not used**. Standard 0V - 3.3V input levels should be used for the TTL inputs. Do not exceed 3.3V**

	Sample0	Sample1	Sample2	Sample 3	….. etc
Data bit 31:	TTL 0(s=0)	TTL 0(s=1)	TTL 0(s=2)	TTL 0(s=3)	
Data bit 30:	TTL 1(0)	TTL 1(1)	TTL 1(2)	TTL 1(3)	
Data bits 29-16:	Analog input IN0(0)	Analog input IN0(1)	Analog input IN0(2)	Analog input IN0(3)	
Data bit 15:	TTL 2(0)	TTL 2(1)	TTL 2(2)	TTL 2(3)	
Data bit 14:	TTL 3(0)	TTL 3(1)	TTL 3(2)	TTL 3(3)	
Data bits 13-0:	Analog input IN1(0)	Analog input IN1(1)	Analog input IN1(2)	Analog input IN1(3)	

Figure 14.2. In dual channel mode, the four TTL bits are shown, above the MS bit of analog data in each sample. The two sampled channels, along with the two TTL bits above each are contained in each 32-bit longword of data sent to the host system, as shown above.

Data bit 31:	TTL 0(s=0)	TTL 0(s=2)	TTL 0(s=4)	TTL 0(s=6)	
Data bit 30:	TTL 1(0)	TTL 1(2)	TTL 1(4)	TTL 1(6)	
Data bits 29-16:	Analog input IN0(0)	Analog input IN0(2)	Analog input IN0(4)	Analog input IN0(6)	
Data bit 15:	TTL 0(s=1)	TTL 0(3)	TTL 0(5)	TTL 0(7)	
Data bit 14:	TTL 1(1)	TTL 1(3)	TTL 1(5)	TTL 1(7)	
Data bits 13-0:	Analog input IN0(1)	Analog input IN0(3)	Analog input IN0(5)	Analog input IN0(7)	

Figure 14.3. In single channel mode, in which only IN0 is specified to be acquired, the two TTL bits TTL3 and TTL2, are shown, above the MS bit of analog data for each of the two successive analog samples of IN0 contained in each 32-bit longword of data sent to the host system.

Data bit 31:	TTL 2(s=0)	TTL 2(s=2)	TTL 2(s=4)	TTL 2(s=6)	
Data bit 30:	TTL 3(0)	TTL 3(2)	TTL 3(4)	TTL 3(6)	
Data bits 29-16:	Analog input IN1(0)	Analog input IN1(2)	Analog input IN1(4)	Analog input IN1(6)	
Data bit 15:	TTL 2(s=1)	TTL 2(3)	TTL 2(5)	TTL 2(7)	
Data bit 14:	TTL 3(1)	TTL 3(3)	TTL 3(5)	TTL 3(7)	
Data bits 13-0:	Analog input IN1(1)	Analog input IN1(3)	Analog input IN1(5)	Analog input IN1(7)	

Figure 14.4. In single channel mode, in which only IN1 is specified to be acquired, the two TTL bits TTL1 and TTL0, are shown, above the MS bit of analog data for each of the two successive analog samples of IN1 contained in each 32-bit longword of data sent to the host system.

TTL bits are captured only during non-averaging modes for AD14-400x2 and AD14-500x2. If averaging, leave the TTL bits unconnected.

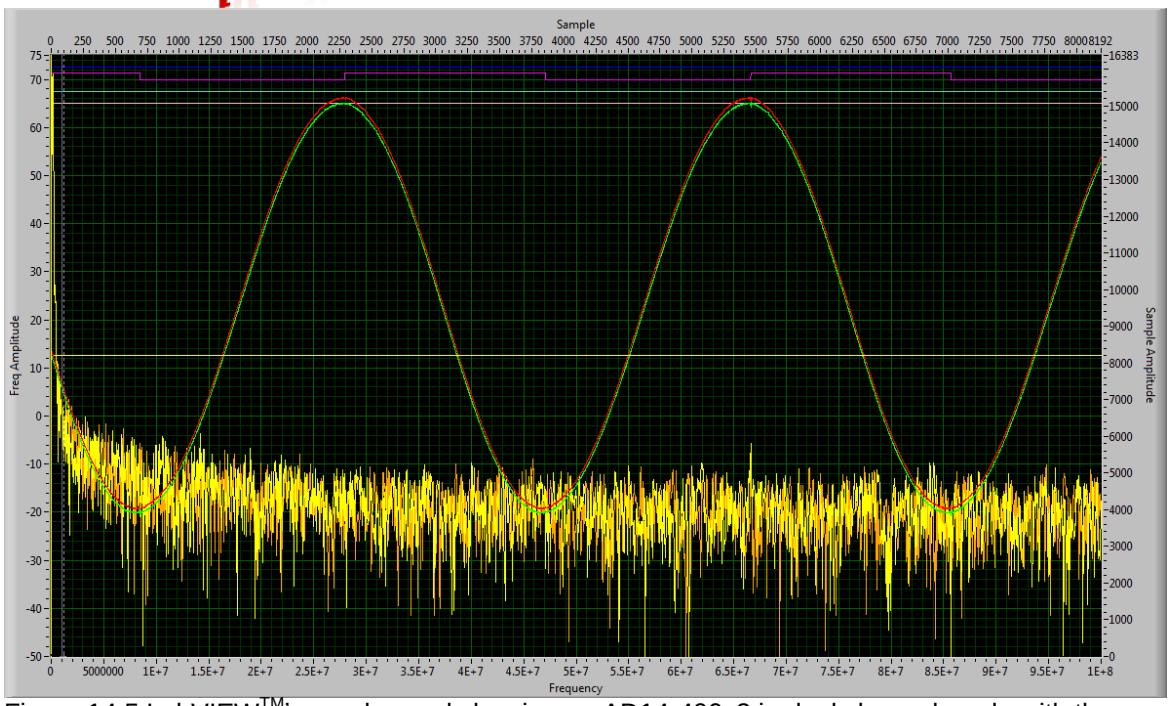


Figure 14.5 LabVIEW™'s graph panel showing an AD14-400x2 in dual channel mode with the TTL signals embedded the top of the graph.

The standard program will keep these TTL signals on the top of the graph, assuming the Sample Amplitude range is large enough to display them. The TTL signals on the graph should be considered arbitrary high and low values.

16. TTL Input Panel for AD12-1800 models

The AD12-1800 model allows concurrent high speed acquisition of up to Four TTL signals, at the same rate as, and time aligned with, the A/D sampling. This feature is useful for correlation of analog/RF signals and the TTL control signals in the system. For example, a rotating RADAR antenna's position may be monitored using the TTL inputs, while the received RF signal is concurrently acquired by the two high-bandwidth analog inputs. These TTL bits are easily inputted to the AD14 board via the small TTL boardlet and uDB26 cable provided with these boards. One end of the cable should be connected to the installed data acquisition card, and the other end should be connected to the TTL boardlet shown in Figure 14.1 above.

	Sample0	Sample1	Sample2	Sample 3	….. etc
Data bit 31:	TTL 0(s=0)	TTL 0(s=1)	TTL 0(s=2)	TTL 0(s=3)	
Data bit 30:	TTL 1(0)	TTL 1(1)	TTL 1(2)	TTL 1(3)	
Data bits 27-16:	Analog input IN0(0)	Analog input IN0(1)	Analog input IN0(2)	Analog input IN0(3)	
Data bit 15:	TTL 2(0)	TTL 2(1)	TTL 2(2)	TTL 2(3)	
Data bit 14:	TTL 3(0)	TTL 3(1)	TTL 3(2)	TTL 3(3)	
Data bits 11-0:	Analog input IN1(0)	Analog input IN1(1)	Analog input IN1(2)	Analog input IN1(3)	

Figure 14.2. In dual channel mode, the four TTL bits are shown, above the MS bit of analog data in each sample. The two sampled channels, along with the two TTL bits above each are contained in each 32-bit longword of data sent to the host system, as shown above.

Data bit 31:	TTL 0(s=0)	TTL 0(s=2)	TTL 0(s=4)	TTL 0(s=6)	
Data bit 30:	TTL 1(0)	TTL 1(2)	TTL 1(4)	TTL 1(6)	
Data bits 27-16:	Analog input IN0(0)	Analog input IN0(2)	Analog input IN0(4)	Analog input IN0(6)	
Data bit 15:	TTL 0(s=1)	TTL 0(3)	TTL 0(5)	TTL 0(7)	
Data bit 14:	TTL 1(1)	TTL 1(3)	TTL 1(5)	TTL 1(7)	
Data bits 11-0:	Analog input IN0(1)	Analog input IN0(3)	Analog input IN0(5)	Analog input IN0(7)	

Figure 14.3. In single channel mode, in which only IN0 is specified to be acquired, the two TTL bits TTL3 and TTL2, are shown, above the MS bit of analog data for each of the two successive analog samples of IN0 contained in each 32-bit longword of data sent to the host system.

Data bit 31:	TTL 2(s=0)	TTL 2(s=2)	TTL 2(s=4)	TTL 2(s=6)	
Data bit 30:	TTL 3(0)	TTL 3(2)	TTL 3(4)	TTL 3(6)	
Data bits 27-16:	Analog input IN1(0)	Analog input IN1(2)	Analog input IN1(4)	Analog input IN1(6)	
Data bit 15:	TTL 2(s=1)	TTL 2(3)	TTL 2(5)	TTL 2(7)	
Data bit 14:	TTL 3(1)	TTL 3(3)	TTL 3(5)	TTL 3(7)	
Data bits 11-0:	Analog input IN1(1)	Analog input IN1(3)	Analog input IN1(5)	Analog input IN1(7)	

Figure 14.4. In single channel mode, in which only IN1 is specified to be acquired, the two TTL bits TTL1 and TTL0, are shown, above the MS bit of analog data for each of the two successive analog samples of IN1 contained in each 32-bit longword of data sent to the host system.

17. APPENDIX – Installing Clock/Trigger Splitter Boards

17.1 Installing the ADSPLTB4 Clock/Trigger Splitter

The ADSPLTB4 is an optional clock/trigger splitter boards that can, from a single clock and optional trigger input, generate as many as four matched clock and trigger outputs for concurrently triggering and running up to four boards. Powered by a "wall-cube" power supply (included), the ADSPLTB4 boards are connected via short SMA-to-SMA cables to the clock and trigger inputs on boards that are to be run concurrently

To install the ADSPLITB4 board, make the following cable connections:

1) Connect the TRIG0 (and TRIG1, 2 and 3, if used) outputs of the ADSPLTB4 to the TRIGGER inputs on the boards you wish to use. Be sure that the cables used are as short as possible (less than 1 foot recommended) and matched to within ¼". Also, check that all SMA cable connectors are firmly hand-tightened onto their respective jacks.

2) Connect the CLK0 (and CLK1, 2 and 3, if used) outputs of the ADSPLTB4 to the CLK inputs on the boards you wish to use. Be sure the cables used are short and matched to within ¼". Check that all SMA cable connectors are firmly hand-tightened.

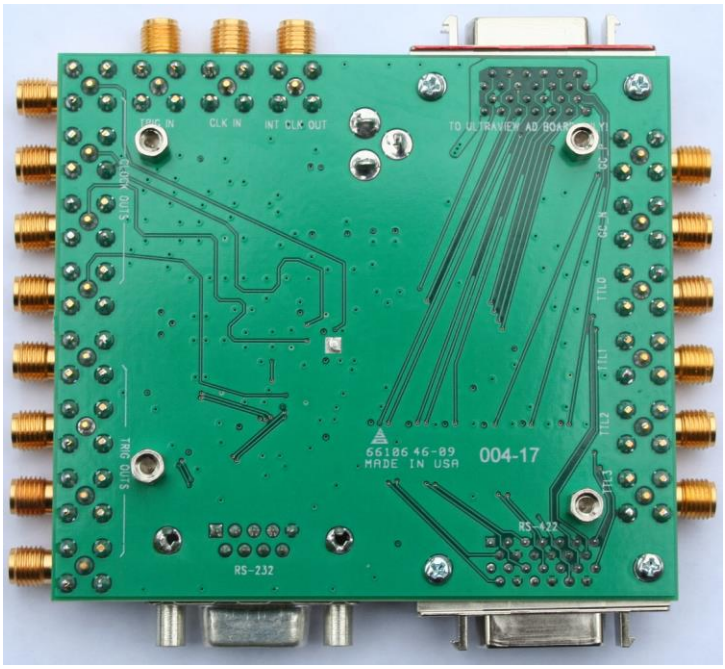
3) Connect the input clock source (0dBm amplitude) to the ADSPLTB4's "CLOCK IN" jack.

4) Plug the +5V adapter's cord into the ADSPLTB4's "DC5V IN" jack. Only the included 5V regulated DC (center + terminal) adapter should be used with the ADSPLTB4.

5) Plug the +5V AC adapter into a standard 120VAC outlet.

After installing the ADSPLTB4 board, the acquire disable LED on boards connected to the ADSPLTB4 should change in response to the single external trigger input, to verify this try connecting a very low frequency (a few tens of hertz is OK) square wave to the ADSPLTB4's trigger input.

17.2 Installing The TTL I/O, RS232-RS422, Clock/Trigger Splitter



The TTL I/O, RS232-RS422, Clock/Trigger Splitter.

This board connects to an Ultraview PCIe main board via cable using the 26 pin connector marked: TO ULTRAVIEW A/D BOARD ONLY!". **Do not use the connector market RS-422 for this purpose**! The board allows 4 TTL inputs to be captured along with 14 bit data, on AD14-400x2 and AD14-500x2 models, by connecting the desired external TTL signals to the TTL3, TTL2, TTL1 and TTL0 SMA jacks. TTL signals TTL1 and TTL0 are sampled as bits 15 and bit 14, occupying the most significant two bits of the 16-bit word containing the data from analog channel IN1. Similarly, TTL signals TTL3 and TTL2 are sampled as bits 15 and bit 14, occupying the most significant two bits of the 16-bit word containing the data from analog channel IN0, as shown below:

See Figures 14.2 and 14.3 for TTL output format for AD14-400x2 and AD14-500x2.

There are two additional unused TTL SMA jacks, GC_N and GC_P which are connected to global clock input/outputs on the PCIe main board's FPGA. These TTL I/O are shown on the right hand side (RHS) of the figure above.

The 26 pin digital connector which connects the PCIe main board and optionally powers this board is seen on the top RHS of this board. **This connector is shown with a red stripe as the 26 pin connector on the PCIe main board must only be connected to this connector to prevent a power short.**

The bottom RHS of this board has the same type of 26pin connector, but must not be connected to the PCIe main board. This connector is labeled RS-422 and contains differential RS422 transceivers. The bottom LHS of the board has a DB9 connector with RS232 serial transceivers.

The top LHS of the board has the SMA connectors for the TTL trigger in, clock in, and clock out. The LHS of the board has 4 synchronized trigger outputs and 4 co-phase clock outputs that are buffered versions of the clock in. The clock in SMA must always be driven, if the internal clock is to be used then the user must connect the clock out SMA to the clock in SMA with a short cable.

TTL bits are captured only during non-averaging modes for AD14-400x2 and AD14-500x2. If averaging, leave the TTL bits unconnected.

18. APPENDIX – Host Uploadable Firmware

18.1 Creating SVF files using Xilinx iMPACT™

Creation of SVF files is possible using the current version of Xilinx iMPACT™. It is important that care is taken when creating new SVF files if the user does not have a Xilinx™ programming cable. Reprogramming the onboard PROM using SVF files requires working firmware.

Programming the PROM with an incomplete, non-functional or mis-targeted design will likely require that the PROM be programmed with a Xilinx™ programming cable.

This procedure is only supported if the user starts with Ultraview supplied Xilinx iMPACT™ and Xilinx ISE™ project files, and has not modified any of the project settings.

1. Generate a programming file in Xilinx ISE™
2. Right click the background in the “PROM File Formatter” window in Xilinx iMPACT™, and select “Add Xilinx Device.” Navigate to the BIT file generated in step 1 and click “Open”.
3. In the “PROM File Formatter” window, double-click “Generate File...”
4. Switch to the “Boundry Scan” window
5. From the menu bar, select Output → SVF File → Create SVF file
6. The Ultraview PROM programming application requires that the name of the SVF file is “ad83000x.svf”. Enter “ad83000x” in the “Create a New SVF File” window and click “Save”
7. Right click on the Xilinx™ part in the “Boundry Scan” window, and choose “Set Programming Properties”
8. Set the following options in the “Device Programming Properties” window:

- Uncheck “Verify”
- Uncheck “Load FPGA”
- Select PROM is configuration master (with 40MHz internal clock)
- Enter the 8 hex digit representation of your device's serial number in the PROM usercode field

9. Select the Xilinx™ part in the “Boundry Scan” window, and double click on the “Program” process in the iMPACT™ Processes list.
10. Once the process completes and the “SVF Program Succeded” box appears, select Output → SVF File → Stop Writing to SVF file from the menu bar.
11. The SVF created in step 5 will now contain the information needed to reprogram the PROM using the Ultraview supplied application “load_svf”. Instructions for loading the PROM using the new SVF file are contained within the next section.

18.2 Instructions for reprogramming the FPGA using SVF files

WARNING: Interruption of load_svf will corrupt the firmware, and your board may need to be programmed using a Xilinx™ programming cable.

18.2.1 Instructions for Windows Vista™ or XP™[

1. Copy ad83000x.svf to the "precompliled_apps" subdirectory in the Ultraview installation directory. This directory will contain the program “load_svf.exe”; **“load_svf.exe” always loads the SVF file named “ad83000x.svf”.**

2. Open the command prompt (In Windows Vista, navigate to Start Menu → All Programs → Accessories → Command Prompt. In Windows XP, navigate to Start Menu → Run. Enter “cmd” and press return)

3. Change directory to the "precompliled_apps" directory containing load_svf.exe in the command prompt. The path to your installation directory is variable, and chosen when the Ultraview software is first installed.)

4. Execute load_svf.exe by typing “load_svf” in the command prompt.

5. The software will now upload the new firmware to the PROM on the the board. This will take a while; depending on the system it may take between 2 and 20 minutes. **Do not interrupt the upload.** Interrupting the upload will corrupt the firmware; if the firmware is corrupted the board may need to be programmed using a Xilinx™ programming cable.

6. When the message “Programming Took __min __sec” appears, and the command prompt “....\AD8-3000_firmware_swap>” appears, programming is finished.

7. Shut down your system. **Note: It is important to shut your machine down as oppose to restarting, as power cycling your system will configure the FPGA with the new firmware contained in the PROM.**

8. Turn on your system. Your board will now be programmed with the new firmware.

18.2.2 Instructions for Linux (64-bit)

1. Copy ad83000x.svf to the Ultraview installation directory /uvdma/example_programs/. This directory will contain the program “load_svf”; **“load_svf” always loads the SVF file named “ad83000x.svf”.**

2. Open a terminal in the example_programs directory.

3. Run load_svf by typing “./load_svf” in the console.

4. The software will now upload the new firmware to the PROM on the AD8-3000. This will take a while; depending on the system it may take between 3 and 30 minutes. **Do not interrupt the upload.** Interrupting the upload will corrupt the firmware; if the firmware is corrupted the board may need to be programmed using a Xilinx™ programming cable.

5. When the message “Programming Took __min __sec” appears, and the command prompt “....\example_programs#” appears, programming is finished.

6. Shut down your system. **Note: It is important to shut your machine down as oppose to restarting, as power cycling your system will configure the FPGA with the new firmware contained in the PROM.**

7. Turn on your system. Your board will now be programmed with the new firmware.

19. APPENDIX – Firmware update using programming cable

1. Place the_top_mod.bit a system running the latest version of Xilinx iMPACT™. The BIT file is the PROM file containing the firmware update. Create a new project, and select “Prepare a PROM File”.
2. In the "PROM File Formatter" window, select “Xilinx Flash/PROM”. Under PROM Family, select “Platform Flash”. For the Device (bits), examine the back of the card for the correct PROM type (either xcf16p or xcf32p). The “Output File Name” and “Output File Location” can be of your choice. Press “OK”.
3. A prompt will appear to load the desired BIT file to be generated. Browse and select the BIT file provided. Say no to any revisions.
4. Under the "iMPACT Processes" window double-click on "Generate File". The MCS file generated will be created with the “Output File Name” in the “Output File Location” previously specified.
5. Under “iMPACT Flows” double-click "Boundary Scan". Right click on the part image and select "Assign New Configuration File". Browse to and select the MCS file you just created. If prompted, select the PROM type you selected earlier.
6. With the programming cable connected to the system running iMPACT™ connect the programming cable's ribbon cable to the programming header on the board. **Ensure that the red stripe on the ribbon cable is connected to pin 1 on the programming header, as shown below. Improper connection could damage the board.**
7. Power up the system containing the board to be programmed. Booting the system into the BIOS is the safest thing to do.
8. Right-click on the part image again and select "Set Programming Properties". Change the "PROM/CoolRunner-II Usercode" field to the hexadecimal representation of your board's serial number. E.g. serial number 1000 decimal becomes 000003e8. Check “Verify”, “Design-Specific Erase Before Programming”, “Load FPGA”, and “During Configuration: PROM is Configuration Master” and select “Internal Clock (40MHz)”. Press “OK”.
9. Under the "iMPACT Processes" window double-click on "Program". Wait until the operation completes, power off the system containing the board, remove the programming cable, and then restart the system. The board will now contain the new firmware and is ready-to-use.

Programming cable orientation.

20. APPENDIX – ADC Gain/Offset/Bias Calibration

Normally, users should not need to recalibrate In the Windows releases, the file “ultra_config.dat” in the “build” directory contains all the serial numbers, board configurations, and calibration data of all distributed A/D boards. Similarly for the Linux release, the “ultra_config.dat” file is in the “example programs” folder. The first few lines should describe all of the calibration parameters for offsets, gains, bias, and phase shift.

--(Serial Number)
ADC_RES= (2 digits, base 10) (required always) (ADC bit resolution)
ADC_CHAN= (2 digits, base 10) (required always) (Number of ADC channels)
DAC_RES= (2 digits, base 10) (required always) (DAC bit resolution)
DAC_CHAN= (2 digits, base 10) (required always) (Number of DAC channels)

ADC2OFF= (2 digits, base 16) (only required for 8-bit boards) (00-> no offset, FF-> maximum offset)
ADC3OFF= (2 digits, base 16) (only required for 8-bit boards) (00-> no offset, FF-> maximum offset)
ADC2OFFNEG= (1 digit, base 2) (only required for 8-bit boards) (1-> offset is negative, 0-> offset is positive)
ADC3OFFNEG= (1 digit, base 2) (only required for 8-bit boards) (1-> offset is negative, 0-> offset is positive)
ADC2FSR= (3 digits, base 16) (only required for 8-bit boards) (Gain adjustment, 000 to 1FF)
ADC3FSR= (3 digits, base 16) (only required for 8-bit boards) (Gain adjustment, 000 to 1FF)

ADC08D1520= (1 digits, base 2) (only required for 8-bit boards) (Set to 1 if board has ADC08D1520 parts)
CLK500PHS= (3 digits, base 16) (only required for 8-bit boards) (National 8-bit ADC clock adjust at 500MHz clock)
CLK1000PHS= (3 digits, base 16) (only required for 8-bit boards) (National 8-bit ADC clock adjust at 500MHz clock)
SHIFTADC2=1 (1 digits, base 2) (only required for 8-bit boards) (National 8-bit ADC phase shift ADC2 clock or ADC3 clock)

ADC2OFF_Q= (2 digits, base 16) (only required for 8-bit ADC08D1520 boards) (00-> no offset, FF-> maximum offset)
ADC3OFF_Q= (2 digits, base 16) (only required for 8-bit ADC08D1520 boards) (00-> no offset, FF-> maximum offset)
ADC2OFFNEG_Q= (1 digit, base 2) (only required for 8-bit ADC08D1520 boards) (1-> offset is negative, 0-> offset is positive)
ADC3OFFNEG_Q= (1 digit, base 2) (only required for 8-bit ADC08D1520 boards) (1-> offset is negative, 0-> offset is positive)
ADC2FSR_Q= (3 digits, base 16) (only required for 8-bit ADC08D1520 boards) (Gain adjustment, 000 to 1FF)
ADC3FSR_Q= (3 digits, base 16) (only required for 8-bit ADC08D1520 boards) (Gain adjustment, 000 to 1FF)

ADCGAIN0= (3 digits, base 16) (only required for 14-bit boards) (Gain adjustment, 400 to 700)
ADCGAIN1= (3 digits, base 16) (only required for 14-bit boards) (Gain adjustment, 400 to 700)
ADCOFFS0= (3 digits, base 16) (only required for 14-bit boards) (Offset adjustment, ? to ?)
ADCOFFS1= (3 digits, base 16) (only required for 14-bit boards) (Offset adjustment, ? to ?)
ADCOFFS2= (3 digits, base 16)
ADCOFFS3= (3 digits, base 16)
ADCBIAS0= (3 digits, base 16) (only required for 14-bit boards) (Bias current adjustment, ? to ?)
ADCBIAS1= (3 digits, base 16) (only required for 14-bit boards) (Bias current adjustment, ? to ?)
ADCBIAS2= (3 digits, base 16)
ADCBIAS3= (3 digits, base 16)

ADC12D2000= (2 digits, base 2)(only used for AD12-1800)
ADC12D2000_DESI_Q_OFFSET= (3 digits, base 16)(Q offset adjustments to match when in single channel I)
ADC12D2000_DESQ_I_OFFSET= (3 digits, base 16)(I offset adjustments to match when in single channel Q)
ADC12D2000_DESIQ_I_OFFSET= (3 digits, base 16)(I offset adjust when IQ are electrically tied in SCM)
ADC12D2000_DESIQ_Q_OFFSET= (3 digits, base 16)(Q offset adjust when IQ are electrically tied in SCM)

ISLA_ADCX_GAIN_COARSE0= (4 digits, base 16) (only used for AD14-500/AD16-250 boards)
ISLA_ADCX_GAIN_MEDIUM0= (2 digits, base 16) (only used for AD14-500/AD16-250 boards)
ISLA_ADCX_GAIN_FINE0= (2 digits, base 16) (only used for AD14-500/AD16-250 boards)
ISLA_ADCX_GAIN_COARSE1= (4 digits, base 16) (only used for AD14-500/AD16-250 boards)
ISLA_ADCX_GAIN_MEDIUM1= (2 digits, base 16) (only used for AD14-500/AD16-250 boards)
ISLA_ADCX_GAIN_FINE1= (2 digits, base 16) (only used for AD14-500/AD16-250 boards)
(Refer to Figure 18.1 for proper input values)

Where X = 0,1,2,3 the channel numbers on the board

TABLE 6. COARSE GAIN ADJUSTMENT

0x22[3:0] core 0 0x26[3:0] core 1	NOMINAL COARSE GAIN ADJUST (%)
Bit3	+2.8
Bit2	+1.4
Bit1	-2.8
Bit0	-1.4

TABLE 7. MEDIUM AND FINE GAIN ADJUSTMENTS

PARAMETER	0x23[7:0] MEDIUM GAIN	0x24[7:0] FINE GAIN
Steps	256	256
-Full Scale (0x00)	-2%	-0.20%
Mid-Scale (0x80)	0.00%	0.00%
+Full Scale (0xFF)	+2%	+0.2%
Nominal Step Size	0.016%	0.0016%

Figure 18.1 ISLA216P25/ISLA214P50 Coarse, Medium, and Fine Gain Adjustment
http://www.intersil.com/content/dam/Intersil/documents/fn75/fn7574.pdf

For AD8-3000 boards:
Adjust ADC2OFF/ADC3OFF so that a open input gives a 50% 127/128 distribution.
Adjust ADC2FSR/ADC3FSR so that a 750mVpp 10.1MHz input is just short of clipping when the internal 1000MHz clock is used.
Adjust CLK500PHS so that there is no phase mismatch between channels with external 500MHz clock and 2002 MHz input.
Adjust CLK1000PHS so that there is no phase mismatch between channels with internal 1000MHz clock and 2002 MHz input.
Set SHIFTADC2=0/1 to phase ADC2 versus ADC3.

For AD8-1500 boards:
Adjust ADC3OFF/ADC3OFF_Q so that a open input gives a 50% 127/128 distribution.
Adjust ADC3FSR/ADC3FSR_Q so that a 750mVpp 10.1MHz input is just short of clipping when the internal 1000MHz clock is used.

Adjust CLK500PHS so that there is no phase mismatch between channels with external 500MHz clock and 2002 MHz input.
Adjust CLK1000PHS so that there is no phase mismatch between channels with internal 1000MHz clock and 2002 MHz input.
Set SHIFTADC2=0/1 to phase ADC2 versus ADC3.

For AD12-1800 boards:

Set to dual channel mode
Adjust ADC3OFF/ADC3OFF_Q so that an open input gives a 50% 2047/2048 distribution.
Adjust ADC3FSR/ADC3FSR_Q so that a 750mVpp 10.1MHz input is just short of clipping when the internal 1000MHz clock is used.

Set to single channel mode, channel 0

Adjust ADC12D2000_DESQ_I_OFFSET so that an open input gives a 50% 2047/2048 distribution. Check FFT.

Set to single channel mode, channel 1
Adjust ADC12D2000_DESI_Q_OFFSET so that an open input gives a 50% 2047/2048 distribution. Check FFT.

Set to DESIQ
Adjust DESIQ_I_OFFSET and DESIQ_Q_OFFSET so that an open input gives a 50% 2047/2048 distribution. Check FFT.

For AD14-400 boards:
Adjust ADCXOFF so that a shorted input gives a midscale value.
Then adjust ADCXBIAS so that an open input gives a midscale value.
Then adjust ADCXFSR so that a 750mVpp 1.1MHz input is just short of clipping, FSR must be in range 0x400-0x700?

For AD14-500 boards:
Adjust ADCXOFF so that a shorted input gives a midscale value.
Then adjust ADCXBIAS so that an open input gives a midscale value.
Then adjust ISLA_ADCX_GAIN_COARSEX, ISLA_ADCX_GAIN_MEDIUMX, and ISLA_ADCX_GAIN_FINEX so that all channels are aligned (where X = 0,1,2,3 the channel numbers on the board, and Y = 0,1 the two cores in each ADC).

For AD16-250 boards:
Adjust ADCXOFF so that a shorted input gives a midscale value.
Then adjust ADCXBIAS so that an open input gives a midscale value.
Then adjust ISLA_ADCX_GAIN_COARSEY, ISLA_ADCX_GAIN_MEDIUMY, and ISLA_ADCX_GAIN_FINEY so that all channels are aligned (where X = 0,1,2,3 the channel numbers on the board, and Y = 0,1 the two cores in each ADC).
.
In LabVIEW, there are controls for adjusting bias, offset, and gains. User must manually input them into “ultra_config.dat” so that it can be used next time the ADCs are calibrated.

21. APPENDIX – DRAM DQS/DQ Calibration

Before delivery, DRAM calibration and gain/offset/bias adjusts are done. When major firmware upgrades are performed off-site, DRAM timing relationships may change. In that situation, recalibration may be required.

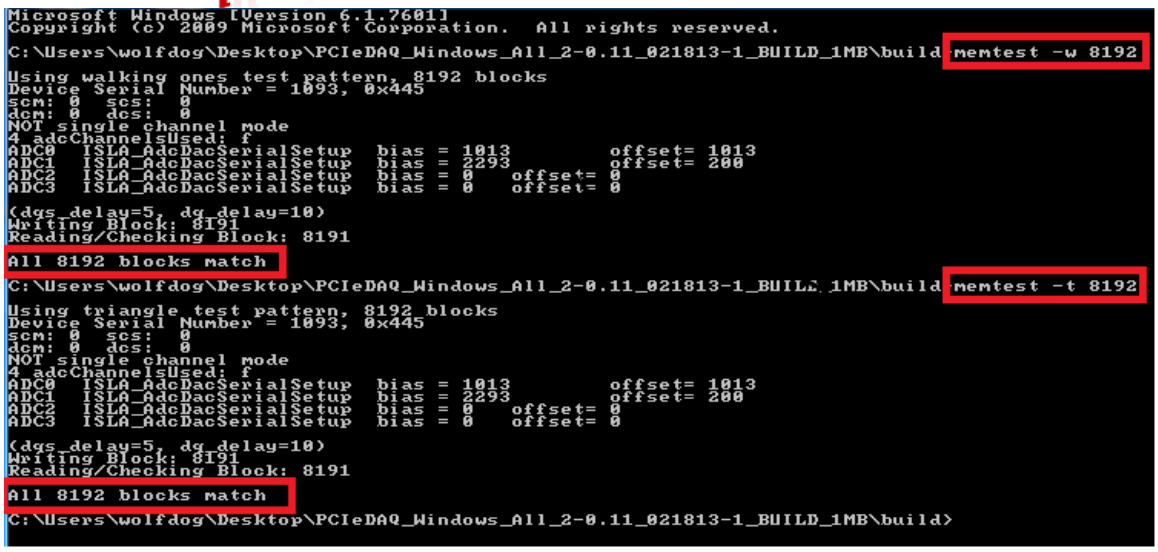
Open a terminal in the “example programs” folder in Linux or the Command Prompt in the “build” directory in Windows.

Step 1: Check to see if calibration is required by typing the following commands:

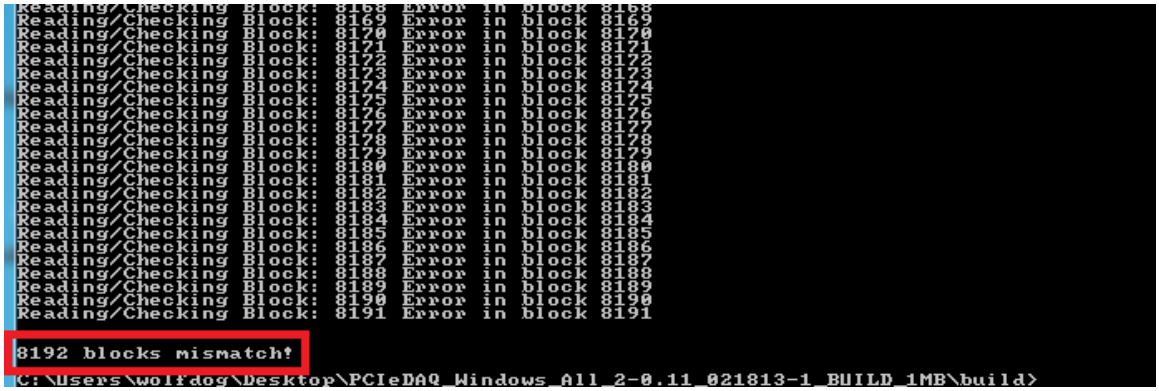
Linux : “./memtest –w 8192”
“./memtest –t 8192”

Windows : “memtest –w 8192”
“memtest –t 8192”

“-w” performs a walking ones test. “-t” performs a triangle test”.



Successful DRAM test. DRAM DQS and DQ values are valid.



Unsuccessful DRAM test. DRAM DQS and DQ calibration required.

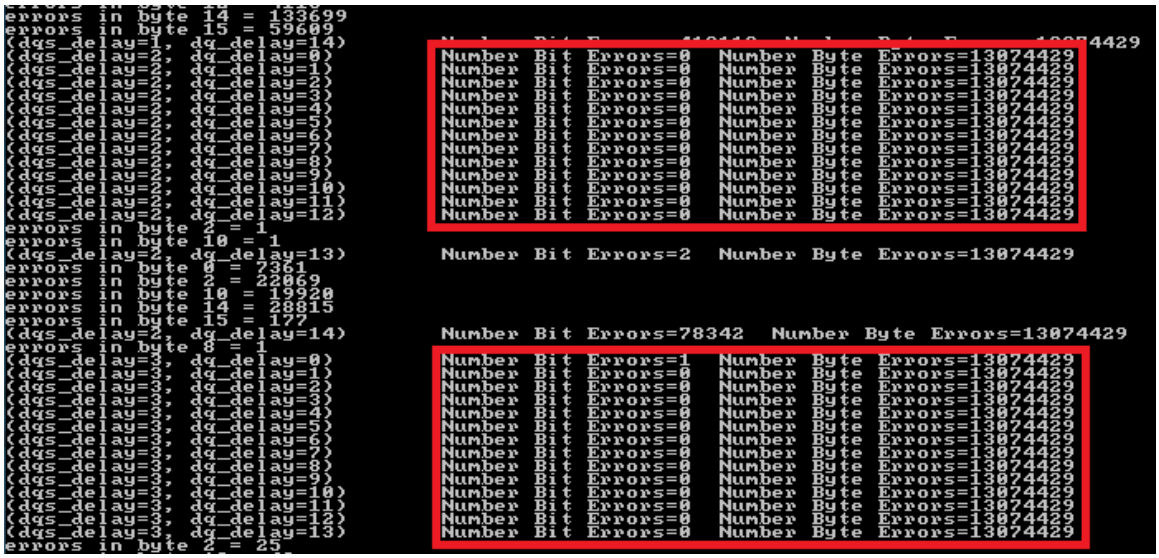
Step 2: If there are any number of block mismatches during either of the two memtests, run a DRAM sweep of DQS and DQ parameters by entering the following line:

Linux : "./memtest –cal –w 32"
Windows : "memtest –cal –w 32"

…

Wait while the sweep runs through all DQS and DQ permutations

…



Output summary of all the DQS and DQ combinations. Combinations where “Number Bit Errors=0” are typically valid.

Step 3: Choose a combination near the center where there are zero bit errors (In this example, DQS=2 and DQ=6 OR DQS=3 and DQ=7 are both good combinations to try).

Step 4: Open “ultra_config.dat” located in either “example programs” (Linux) or “build” (Windows), find your board number, modify/enter the DRAM_DQS and DRAM_DQ values, and Save.


```
--1093
ADC_RES=14
ADC_CHAN=02
DAC_RES=14
DAC_CHAN=00
ADCGAIN0=500
ADCGAIN1=500
ADCOFFS0=3F5
ADCOFFS1=0C8
ADCBIAS0=3F5
ADCBIAS1=8F5
ISLA214P=1
ISLA_ADC0_IDELAY_OFFSET=0b
ISLA_ADC1_IDELAY_OFFSET=04
DRAM_DQS=05
DRAM_DQ=10
```

Step 5: Repeat Steps 1-4 until the DRAM test is always successful. Try different combination values if unsuccessful.

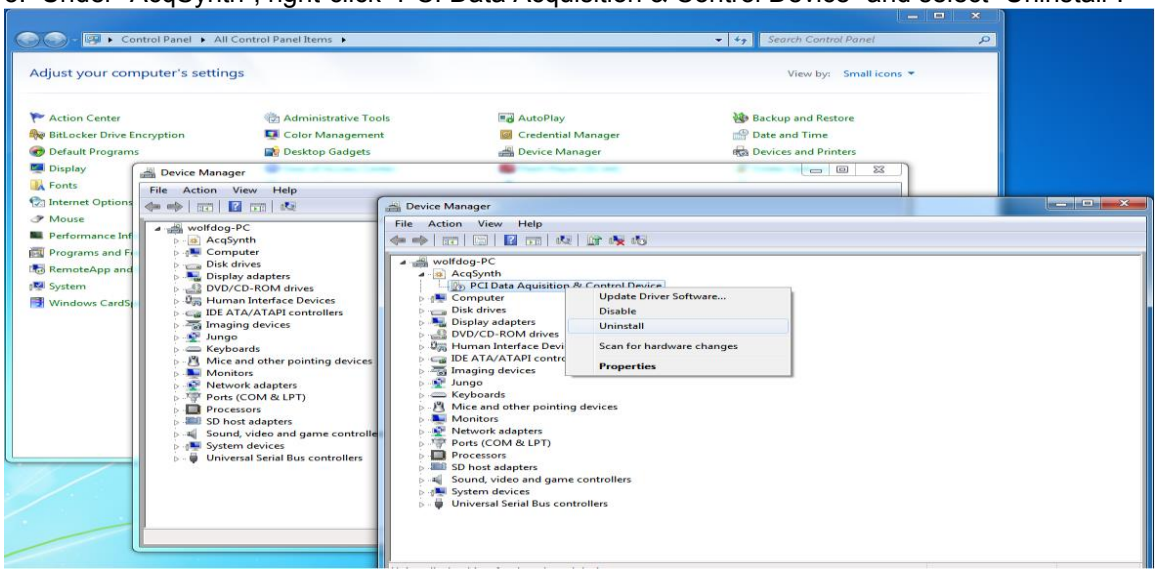
22. Updating Windows 7/8 64-bit Driver

This section describes how to update the Windows 7/8 64-bit driver on a system with a pre-existing driver. Most commonly, users will follow these instructions when they want to install the new signed drivers.

1. In order to recognize the board, boot Windows with “Disabled Driver Signature Enforcement”

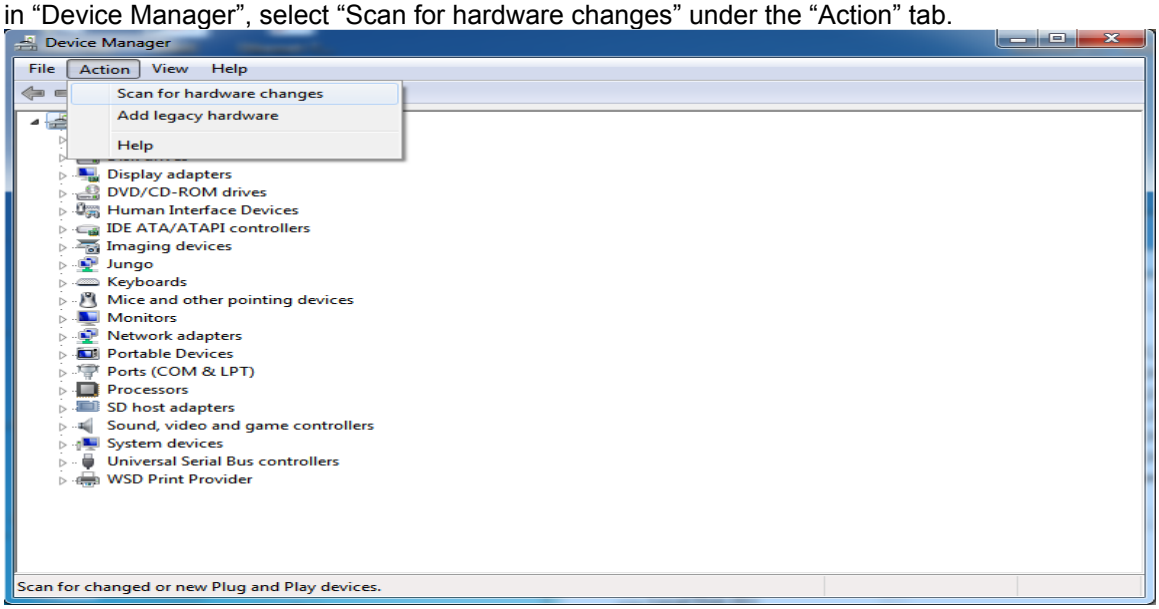
2. Navigate to “Control Panel” => “Device Manager”

3. Under “AcqSynth”, right-click “PCI Data Acquisition & Control Device” and select “Uninstall”.

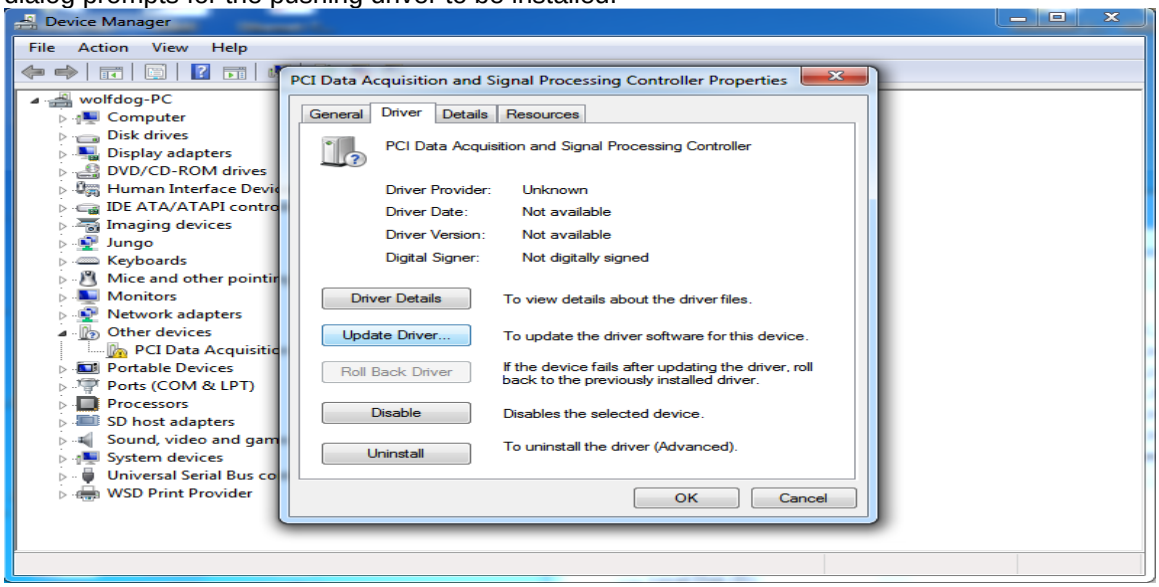


4. A “Confirm Device” dialog should pop-up. Check the box that says “Delete the driver software for this device” and press “OK”.

5. The old driver is now uninstalled. To facilitate the device to be recognized by Windows again, in “Device Manager”, select “Scan for hardware changes” under the “Action” tab.



6. Allow Windows time to search and fail for a device driver. In “Device Manager” under “Other devices”, double-click “PCI Data Acquisition & Control Device”, select “Update Driver”, browse manually to folder in the software release where the 64-bit driver is located. Press “OK” when a dialog prompts for the pushing driver to be installed.



7. The driver should now be installed. A restart may be required before the board can be used.

23. APPENDEX – How to Update Your LabVIEW™ Project

This section is for users who have modified a LabVIEW™ project from a previous release and wish to update their project to work with the latest software release.

There are two ways of merging a project successfully, using components from the new release and merging into the old release, and vice versa. For this tutorial, we will use components from the latest release and merge into the older release.

1) From the latest release, you will need the following items:

A) Folders: **_DllSource**, **AppSource**

B) In the "build" directory: **ultra_config.dat**, **UltraPCIeSetup.xml**

ultra_config.dat = Configuration data for all boards.

C) In Labview PCIe DAQ XXXX / AcqSynth Library where the LabVIEW™ VIs are stored: **Global setup_struct cluster.vi**

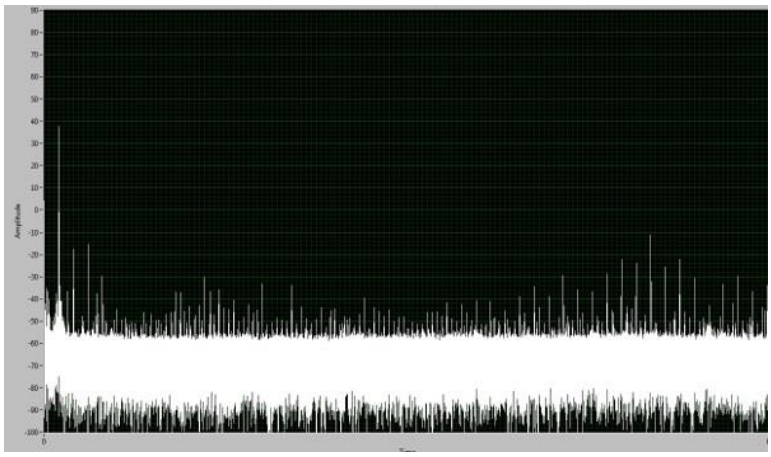
Global setup_struct cluster.vi = LabVIEW's local copy of setup_struct. The size, names, and types need to match the DLL's setup_struct.

2) Replace each item in 1) into their respective locations in the release you wish to merge.

3) Recompile the DLL and the acquire program, and any other programs that you would use the DLL (e.g. memtest, digosc).

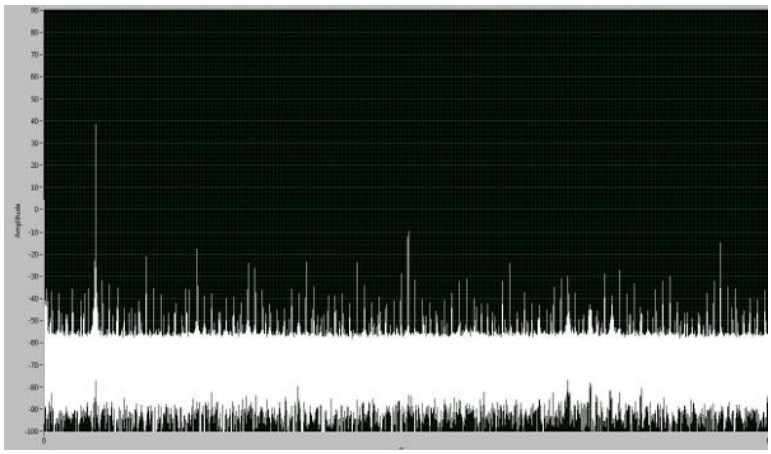
4) Make sure the new setup_struct cluster in the LabVIEW™ project is present, and recompile.

24. APPENDIX – Measurement Data



24.1 AD8-3000 FFT SNR, SFDR

AD8-3000 1MB FFT with a 12MHz Input, 9-15MHz BPF, 2000MSPS



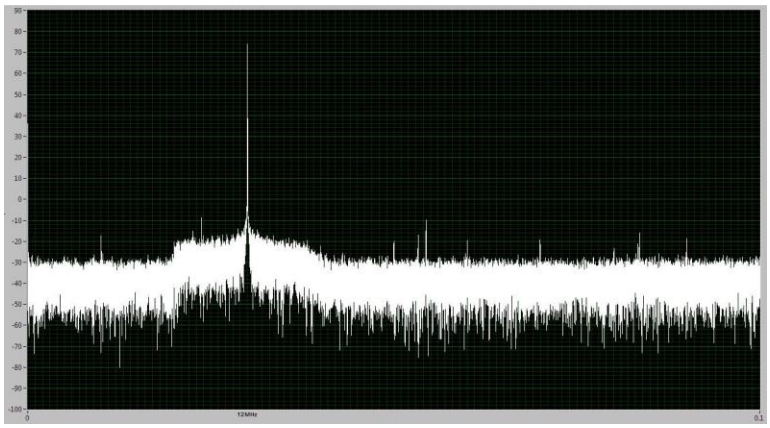
AD8-3000 1MB FFT with a 70MHz Input, 70MHz BPF, 2000MSPS

24.2 AD12-1800 FFT SNR, SFDR

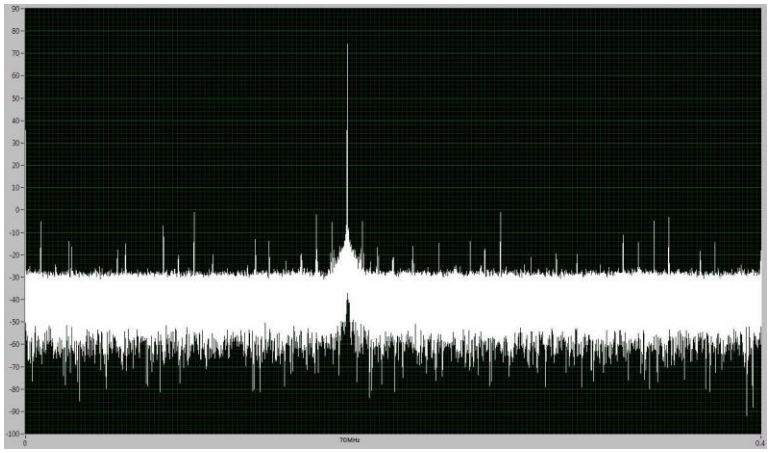
AD12-1800 1MB FFT with a 100MHz Input, 9-15MHz BPF, 500MSPS TBD

AD12-1800 1MB FFT with a 70MHz Input, 70MHz BPF, 500MSPS TBD

24.3 AD14-400 FFT SNR, SFDR



AD14-400 1MB FFT with a 12MHz Input, 9-15MHz BPF, 400MSPS



AD14-400 1MB FFT with a 70MHz Input, 70MHz BPF, 400MSPS

25. APPENDIX – Data Output Format (uvdma.dat)

8-bit Single Channel | [X][M] | where X = channel # and M = sample (1 byte).

[0][0]	[0][1]	[0][2]	[0][3]	[0][4]	[0][5]	…

8-bit Dual Channel | [X][M] | where X = channel # and M = sample (1 byte).

[0][0]	[1][0]	[0][1]	[1][1]	[0][2]	[1][1]	…

14/16-bit Single Channel | [X][M][N] | where X = channel #,
M = sample (2 bytes),
N = byte #, 0 is LSB.

[0][0][0]	[0][0][1]	[0][1][0]	[0][1][1]	[0][2][0]	[0][2][1]	…

14/16-bit Single Channel (Averaging) | [X][M][N] | where X = channel #,
M = sample (4 bytes),
N = byte #, 0 is LSB.

[0][0][0]	[0][0][1]	[0][0][2]	[0][0][3]	[0][1][0]	[0][1][1]	[0][1][2]
[0][1][3]	[0][2][0]	[0][2][1]	[0][2][2]	[0][2][3]	…	…

14/16-bit Dual Channel | [X][M][N] | where X = channel #,
M = sample (2 bytes),
N = byte #, 0 is LSB.

[0][0][0]	[0][0][1]	[1][0][0]	[1][0][1]	[0][1][0]	[0][1][1]	[1][1][0]
[1][1][1]	[0][2][0]	[0][2][1]	[1][2][0]	[1][2][1]	…	…

14/16-bit Dual Channel (Averaging) | [X][M][N] | where X = channel #,
M = sample (4 bytes long),
N = byte #, 0 is LSB.

[0][0][0]	[0][0][1]	[0][0][2]	[0][0][3]	[1][0][0]	[1][0][1]	[1][0][2]
[1][0][3]	[0][1][0]	[0][1][1]	[0][1][2]	[0][1][3]	[1][1][0]	[1][1][1]
[1][1][2]	[1][1][3]	…	…	…	…	…

16-bit Quad Channel | [X][M][N] | where X = channel #,
M = sample (2 bytes long),
N = byte #, 0 is LSB.

[0][0][0]	[0][0][1]	[1][0][0]	[1][0][1]	[2][0][0]	[2][0][1]	[3][0][0]
[3][0][1]	[0][1][0]	[0][1][1]	[1][1][0]	[1][1][1]	[2][1][0]	[2][1][1]
[3][1][0]	[3][1][1]	…	…	…	…	…

16-bit Quad Channel (Averaging) | [X][M][N] | where X = channel #,
M = sample (4 bytes long),
N = byte #, 0 is LSB.

[0][0][0]	[0][0][1]	[0][0][2]	[0][0][3]	[1][0][0]	[1][0][1]	[1][0][2]
[1][0][3]	[2][0][0]	[2][0][1]	[2][0][2]	[2][0][3]	[3][0][0]	[3][0][1]
[3][0][2]	[3][0][3]	…	…	…	…	…

26. Known Issues

The following issues have been noted and will be addressed at a later time:

1. For some boards, the first 64 samples occasionally contain a single sample glitch in data.

2. When using the analog waveform trigger or the heterodyne trigger under LabVIEW™, TTL Trigger Edge Enable must be set.

3. There is a LabVIEW™ bug where the checkbox for the first channel does not work. Instead, left-click on the plot icon and deselect “Plot Visible”.

4. There is a LabVIEW™ bug where the plot legend retains all plots in the list, even if there is no data in those channels. The superfluous plots should be ignored.

5. Errors 63 and 66 are TCP/IP read and write failures in LabVIEW™. Ensure that no firewall or network limitations are in effect.

6. Our A/D boards will freeze if the PC sleeps. All power saving features should be disabled.

7. We have experienced from customers failure to properly boot the board with power supplies less than 500W. We have tested and recommend the following PC configuration:

Asus P8Z77V series motherboard (optional)
Any socket 1155 CPU (we have tested i7-2700,i7-3770)
At least 8GB RAM
At least 500W power supply
Integrated graphics (on motherboard) OK to use.

